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L1 TRIGGER Board VME Address Space for Apr 2015 Run

Monica Tecchio
University of Michigan

This document specifies the VME Address Space defined in the firmware of the L1 TRIGGER board. The L1 TRIGGER board uses only one of the two FPGAs, the XC5VFX70T, which is designed to receive parallel inputs from 16 external SERDES chips, receive and drive a 24-bit daisy-chain from the P3 backplane and connect to the P1 and P2 VME signals. In the May 2013 run, we used version 5.4 of the L1 Trigger Virtex5 firmware. A second Xilinx FPGA (XC4VFX12) is installed on the board but is not used for any of the L1 Trigger functionality [1]. To fully exploit the improved functionality and added flexibility of this firmware, it should be used with version 7.5 (and above) of the Master MACTRIS firmware.

1 Introduction

The TRIGGER Module revC-v2 has been designed to receive up to 16 fibers running at 2.5Gb/s, deserialize the encoded 8-to-10 bit information via Texas Instruments TLK3101 transceivers and send the parallel 16-bits of data to an on board Virtex 5 Xilinx FPGA. It can also transmit signals out of the fiber connected to input port 7. This 9U board is used both in the L1 Trigger and the L2 Trigger crates. When in the L1(L2) crate, it is connected to the bottom(top) of the two fibers driven by each ADC board, also called L1(L2) fiber. Via the L1 fiber, the ADC sends every 8 ns either the sum of the 14-bit digitized energy over its sixteen channels or a string of 0s and 1s from the peak energy finder. The peak energy finder compares the single channel energy to a predefined threshold and, if found above threshold, marks with a 1 the peak defined as the first sampling with an energy lower that the previous one.

For the trigger modules in the L1 Trigger crate, switches in the firmware allow to select one of the 3 flavors of boards used in the L1 trigger decision: a **CsI L1 Trigger board** receiving ADC energy sums from the CsI detector; a **L1 Veto board** receiving 15 fibers from one or more veto detectors and driving one output fiber to the Master Veto board; and a **Master Veto board** receiving 8 fibers of energy sums from ADCs and 8 fibers of veto trigger fibers from the L1 Veto boards.

In the following we will give an overview of the configuration of the L1 Trigger Crate in section 2 and a description of the main board hardware and firmware features in sections 3. The remaining sections list the registers defined inside the FPGA to simulate and control the

[1] A dummy firmware has to be downloaded to the Virtex4 chip when programming the Virtex5

different board functionalities. Section 4 defines the User Defined Registers in Tables 7, 8 and 9. Section 5 lists the registers used to monitor the incoming fiber energies and the internal sums in Tables **??** and 11, respectively. Finally Section 6 lists the content of the firmware (mostly in schematics entry) sheet by sheet

2 The L1 Trigger Crate

The L1 Trigger Crate is a 21-slot 9U VME64x crate with a modified P2 backplane and a custom-made P3 backplane. The P2 backplane, on top of some standard VME signals, has two sets of differential lines used to distribute the 8ns system clock and the L1A trigger decision to all of the boards in the crate, plus multiple Low Voltage TTL single ended lines used to distribute other DAQ Control signals (see Table 1). Some of them are driven by Open Collector (OC) drivers and can be set true by any board in the system. In the present design, the DAQ Control are generated/received by the Master MACTRIS board, located in slot 12, and distributed to the P2 backplane via by the Slave MACTRIS board, located in slot 2 of the L1 trigger crate.

DAQ Signal	Pin	Level	DAQ Signal	Pin	Level
CLK+	A6	Diff. PECL	L1A_EN	C2	LVTTL
CLK-	A7	Diff. PECL	L1A+	C4	Diff. PECL
BEAM_ON	A9	LVTTL	L1A-	C5	Diff. PECL
SPILL_ON	A10	LVTTL	LIVE	C12	LVTTL
L2A	A12	LVTTL	LIVE_EN	C13	LVTTL
L2A_EN	A13	LVTTL	K0TO_HOLD	C16	LVTTL
K0TO_RESET	A15	LVTTL	K0TO_RUN	C17	LVTTL
K0TO_HALT	A16	LVTTL	L2B(0)	C20	LVTTL
K0TO_RECOVER	A18	LVTTL	L2B(1)	C21	LVTTL
K0TO_SAVE	A20	LVTTL	L2B(2)	C22	LVTTL
K0TO_READ	A21	LVTTL	L2B(3)	C23	LVTTL
K0TO_NOT_EMPTY	A23	OC	L2B(4)	C24	LVTTL
K0TO_FULL	A24	OC	L2B(5)	C25	LVTTL
K0TO_ERROR	A26	OC	RDB(0)	C27	LVTTL
K0TO_DONE	A27	OC	RDB(1)	C28	LVTTL
K0TO_OC_RSVD	A30	OC	RDB(2)	C29	LVTTL
K0TO_RSVD	A31	LVTTL	RDB(3)	C30	LVTTL
			RDB(4)	C31	LVTTL
			RDB(5)	C32	LVTTL

Table 1: List of DAQ Control Signals and mapping to the P2 backplane pin: LVTTL and Differential PECL Signals are generated by MACTRIS and received by the Trigger boards while Open Collector (OC) signals can de driven by any of the Trigger boards and received by MACTRIS. All of the signals are negative logic.

The P3 backplane is a custom made backplane designed to connect specific slots in the crate

via daisy-chain. The left and right daisy-chains originate in slot 4 and 20 respectively, and end in slot 12. On the way to slot 12, they connect together slots 4,5,6,9,10,11 and 13,14,15,18,19,20, respectively. The daisy-chain comprises a 24 bit bus, with bit(17:0) reserved for energy signals and bit(23:18) for veto signals.

Five of the six slots in each daisy-chain are reserved for CsI L1 Trigger boards, and cover most of the 2708 crystals comprising the CsI calorimenter. The two outermost slots are used by the left and right Master Veto boards, which are programmed to receive both CsI fibers in inputs 8 and 15 and L1 Veto fibers in inputs 0 and 7. The remaining available slots in the crate (3, 7, 8, 16, 17 and 21) are used by L1 Veto boards which receive a variable number of input fibers from the different veto subdetectors and generate up to 16 independent veto triggers based on comparisons of total or partial energy sums, and total or partial hit multiplicities (i.e. veto hits coincidences in a given sampling), to programmable thresholds. Table 2 summarizes the Trigger boards position in the L1 Trigger Crate and its input fiber connections.

For the May 2013 run, all ADC boards are 125 MHz except for the board digitizing the beam hole veto detectors, which are 500 MHz boards. For 125 MHz boards, hit multiplicity is simply the sum of all hits above threshold seen by the 16 ADC input channels in an 8 ns sample. For 500 MHz boards, the 2 ns digitalized info from the 4 ADC channels is multiplexed into the 16 bits carried by each fiber in the following order: (h_{00},h_{10}, h_{20},h_{30},h_{01},h_{11}...h_{23},h_{33}), where h_{xy} is the hit for channel x of the 2-ns sampling y. Thus hit multiplicity in a 8 ns sample is the logical OR of the underlying 2 ns hits for a given channel. For example, the channel 0 hit multiplicity is calculated as (h_{00}.OR. h_{01}.OR.h_{02}.OR.h_{03}).

Slot	Board Flavor	ADC Crate	Input Port Usage
3	CV L1Veto	A11	0-2, 4-6, 8-10, 12-14
4	Left Master Veto	A5	8-15 (for inputs 0-7, see Table 3)
5	Csi L1TRG	A4	0-15
6	Csi L1TRG	A3	0-15
7	FB-MB L1 Veto(BCV)	A14	0-3
7	FB-MB L1 Veto(FB)	A13	4-5
7	FB-MB L1 Veto(Inner MB)	A14	8-11
7	FB-MB L1 Veto(Outer MB)	A14	12-15
8	NCC Common Veto	A13	0-2
8	NCC Front Veto	A13	4-6
8	NCC Middle Veto	A13	8-10
8	NCC Rear Veto	A13	12-14
9	Csi L1TRG	A2	0-15
10	Csi L1TRG	A1	0-15
11	Csi L1TRG	A0	0-15
13	Csi L1TRG	A10	0-15
14	Csi L1TRG	A9	0-15
15	Csi L1TRG	A8	0-15
16	OEV L1Veto	A11	0-2
17	BH L1 Veto (BHTS)(*)	A15	0-1
17	BH L1 Veto (BHCV)(*)	A15	2-3
17	BH L1 Veto (BHGC)(*)	A15	4-5
17	BH L1 Veto (BHPV)(*)	A15	8-13
18	Csi L1TRG	A7	0-15
19	Csi L1TRG	A6	0-15
20	Right Master Veto	A5	8-15 (for inputs 0-7, see Table 3)
21	Collar L1 Veto(CCO4)	A12	0-3
21	Collar L1 Veto(CCO3)	A12	4-5
21	Collar L1 Veto(CCO5)	A12	8-11
21	Collar L1 Veto(CCO6)	A12	12-15

Table 2: L1 Trigger board slot position and input fiber connections. (*) These are 500 Mhz ADC boards. When testing the new BHCV system, the fibers to slot 17 are disconnected and replaced by: inputs 0-3 for newBHCV1, inputs 8-11 for newBHCV2 and inputs 12-15 for newBHCV3.

3 The L1 Trigger Board and its firmware

The Trigger Board, see Figure 1, is a 9U VME board with connections to the P1,P0,P2 and P3 VME backplanes. The front panel receives sixteen 2.5Gbs fibers from the ADC board via the IN0 thru IN15 Avago optical receivers. The 16 bit of of data every 8 ns coming from the fiber is deserialez in the TLK transceivers and sent to the Virtex 5 FPGA. A second Virtex 4 FPGA is connected to the first via a so called V2V bus comprising 32-bit data, 5-bit address and 8-bit control signal. The Virtex 4 has in turn connections to two DDR2 2-Git memories and to the Ethernet PHY. A 1Gb Ethernet port (ETH1) and a RJ45 connector (CTRL),able to receive the ADC Control Signals generated by the Master MACTRIS ,complete the list of external connections.

For the purpose of preparing and processing data of the L1A Trigger decision, boards in the the L1 Trigger Crate just need to keep data aligned with the 125 MHz system clock (and neither store them on the on-board memories nor read them out via the 1Gb Ethernet port into the data stream). As such, the L1 Trigger board does not need to use the V4 FPGA and all of its firmware is contained in the V5 FPGA. The Virtex5 has two input clocks: CLK125_OSC, connected to a 125 MHz on-board oscillator; and CLK125_IN, connected to the 8 ns system clock, which can be selected via the JP17 jumper to be either the backplane clock (JP17 off) or the front panel clock (JP17 on). The backplane clock is driven by MACTRIS on the P2 backplane as a differential PECL signal over the A6-A7 pins. The front panel clock is also driven by MACTRIS but distributed to external boards by a repeater card, the Fanout board, as a differential LVDS signal via the CTRL front-panel RJ45 connector [2].

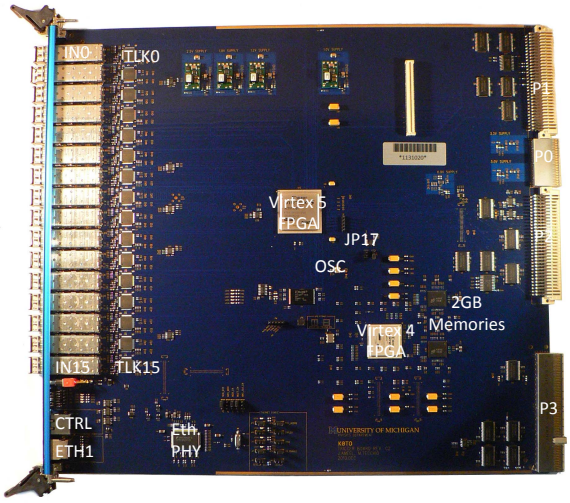

Figure 1: Picture of the TRIGGER board showing the most relevant features.

For firmware versions 3.8 and above, we route the CLK125_OSC clock to the CLK125_OUT0 output clock pin via a fast buffer with 24 mA current drive. This output clock in turn drives

[2]Other two input signals, LIVE and L1A, and an output signal, ERROR, have separate backplane and front panel paths. To select which of the two are used by the firmware, set VME register 0x2c as specified in Table 7.

the master clock input of each TLK3101 chip [3]. The CLK125_IN clock instead is fed into a Phase Lock Loop (PLL) followed by a Digital Clock Manager (DCM) module instantiated inside the Xilinx FPGA fabric. This core generates a zero-delay version of 8 ns system clock (CLK_125) to be used by the rest of the FPGA firmware. This same clock drives, via a fast 24 mA current drive buffer, the CLK125_OUT1 output clock which goes to the P3 daisy-chain signal registered drivers as well to the P2 DAQ Control Signal drivers and receivers.

Fiber	Input Port	Input Fiber Bits	P3 backplane Bit
CV	in_L(0)	(2:0)	out_L(18)
FB-MB (MB)	in_L(1)	(11:0)	out_L(21)
FB-MB (FB)	in_L(1)	(15:12)	out_L(19)
NCC	in_L(2)	(15:0)	out_L(20)
OEV	in_L(3)	(15:0)	out_L(22)
BPCV	in_L(7)	(15:0)	out_L(23)
CC (CC03)	in_R(0)	(7:4)	out_R(18)
CC (CC04)	in_R(0)	(3:0)	out_R(19)
CC (CC05)	in_R(0)	(11:8)	out_R(20)
CC (CC06)	in_R(0)	(15:12)	out_R(21)
BH (BHCV)	in_R(1)	(11:0)	out_R(22)
BH (BHPV)	in_R(1)	(15:12)	out_R(23)

Table 3: Mapping of fibers to Master Veto input ports and P3 backplane bits. The fiber name reflects the name of the L1 Veto module listed in Table 2, except for the BPCV fiber, which is connected directly to the Left Master Veto inputs without going thru any L1 veto boards. In the input port column, L and R stands for Left and Right Master Veto boards, located in slots 4 and 20 respectively. The Input Fiber Bits column lists the maximum number of independent veto trigger bit allocated for each detector. The veto trigger bit definition is specified in Tables 4 and 5. The logical OR of all enabled input fiber bits (see note (n)) drives the P3 backplane bit. This logic is implemented inside the {NEW_MASTER_VETO and the "Master Veto board flavor" bit(20) of register 0xCC select between a bit of the left (out_L) or right (out_R) daisy-chain.

The L1 Trigger board Virtex5 firmware for the May 2013 run has been designed to time-align the sixteen fiber inputs and connect them to different internal logic blocks depending on which

[3]Driving the TLK3101 chips with the local clock, as opposed to the system clock, has proved the key to solving the TLK loss-of-sync problem. This problem showed itself either with frequent synchronization error, or TLK errors, for the data coming into the Trigger board via the ADC L1 and L2 fibers; or with unrecoverable loss-of-synchronization which could be solved only by re-issuing the LIVE signal. These instabilities, probably due to the high jitter of the clock coming into the board via the P3 backplane, would have affected the stability of the data taking in a major way. The quality of the cables used in the propagation of the system clock to the ADC board through the Fanout boards was also affecting the loss-of-problem, again probably because of too high jitter injected in the clock at the transmitting end. Any cable in the KOTO DAQ involved in the system clock transmission, especially the 20ft cable between Master MACTrIS and Master Fanout, is now a CAT 6A Ethernet cable.

flavor of L1 board the user wants to instantiate. The choice of board flavor is done via enables accessible on VME register 0xcc (see Table 8). For the CsI L1 Trigger board, a user programmable number of fibers are connected to the 4 clk latency ENERGY_ADDER block, where the total energy is calculated and passed to bit(17:0) of the P3 backplane daisy-chain; for the Master Veto board, input fibers 0 to 7 are connected to the 4 ck latency NEW_MASTER_VETO block, where a single trigger decision per detector is calculated and passed to bit(23:18) of the daisy-chain; finally for the Veto L1 Trigger board, partial energy and hit multiplicity sums are connected to the 8 clk latency NEW_L1VETO_LOGIC block where up to sixteen independent veto trigger bits per detector are generated (see Table 4). These bits can be individually enabled and driven out of fiber 7 to a predefined input of the Left or Right Master Veto board as specified in Table 3.

One of the firmware basic functionality is to receive the 16-bit energy/veto info from each L1 input fiber and align them with respect to the system LIVE. This is done inside the SUM_ALIGNMENT block, designed to write the 16 input bits into a 64-bit deep FIFO on the fiber recovered clock and hold them inside from the moment the 0xFEFE alignment word is seen [4] until a delayed version of LIVE is generated. At this point, all of the FIFOs are read out simultaneously on the 8 ns the system clock. This alignment word is used to measure the time delay between the first non zero output of the ENERGY_ADDER or NEW_L1VETO_LOGIC block and the first non-zero input seen at daisy-chain input buffer. In order to ensure a proper time delay calculation, the board has to be set in a special "calibration mode". This is because in normal running conditions, the alignment word is masked out.

The firmware provides also multiple diagnostic and programmable features via VME registers to allow, among other things, the disabling of disconnected input fibers, the enabling of extra delay between the input energies, and the monitoring of TLK errors and single-bit errors. In particular, the firmware implements the same 14-bit random sequence which is generated inside the ADC firmware so that a bit-by-bit check of the input fiber energy can be performed at different locations through the firmware. Details on the VME registers used to enable and control all of these features is the subject of the next two sections.

[4] The 0xFEFE word is the first 16-bit word sent from the ADC after LIVE is received. It signals that the active transmission of digitized data via the fiber link has started.

Veto	Output Bit	Description
CV	CV(0)	Peak sum fibers 0 to 15
Front CV	CV(1)	Peak sum fibers 0 to 6
Rear CV	CV(2)	Peak sum fibers 8 to 15
Inner Main Barrel	FB-MB(0)	Peak sum fibers 8 to 11
Outer Main Barrel	FB-MB(1)	Peak sum fibers 12 to 15
Inner+Outer MB	FB-MB(2)	Peak sum fibers 8 to 15
BCV	FB-MB(3)	Peak sum fibers 0 to 3
MB Cosmic	FB-MB(4)	MB Cosmic decision*
FB Peak	FB-MB(12)	Peak sum fibers 4 to 6
FB Gate	FB-MB(13)	Gate sum fibers 4 to 6
FB Hits	FB-MB(14)	Multiplicity sum fibers 4 to 6
NCC Total	NCC(0)	Peak sum fibers 0 to 15
NCC Common+Front	NCC(1)	Peak sum fibers 0 to 6
NCC MIddle+Rear	NCC(2)	Peak sum fibers 8 to 15
NCC Common Peak	NCC(4)	Peak sum fibers 0 to 3
NCC Front Peak	NCC(5)	Peak sum fibers 4 to 6
NCC Middle Peak	NCC(6)	Peak sum fibers 8 to 11
NCC Rear Peak	NCC(7)	Peak sum fibers 12 to 15
NCC Common Gate	NCC(8)	Gate sum fibers 0 to 3
NCC Front Gate	NCC(9)	Gate sum fibers 4 to 6
NCC Middle Gate	NCC(10)	Gate sum fibers 8 to 11
NCC Read Gate	NCC(11)	Gate sum fibers 12 to 15
Special NCC 1	NCC(12)	OR of bits(0/1/14/15) of input fiber 3
NCC Common Only	NCC(13)	Peak sum fibers 0 to 3 .AND.!GATE sum fibers 4 to 6
NCC Middle Only	NCC(14)	Peak sum fibers 8 to 11 .AND.!GATE sum fibers 4 to 6
NCC Deep	NCC(15)	Peak 3-0 .AND. peak 8-11 .AND. peak 12-15 .AND.!GATE 4-6
OEV	OEV(0)	Multiplicity sum fibers 0 to 15
OEV	OEV(1)	Peak sum fibers 0 to 15

Table 4: Description of veto fiber output bits sent from L1 Veto fibers to Master Veto board: **peak** means that the trigger is asserted for *only one clock cycle* corresponding to the sampling with the maximum energy above threshold; **gate** means that the trigger is asserted for *all clock cycles* when the sum is above threshold; **multiplicity** means that the sum of *all single channel above the threshold*, as calculated inside the ADC board, is used to assert the trigger. The Output Bit label reflects the name of the L1 Veto module listed in Table 3. Each of these bits represent a special trigger made to of the specific veto detector signals. The logic used to generate these triggers is implemented inside the NEW_L1VETO_LOGIC block except for FB-MB(4), which is implemented inside the MB_COSMIC_LOGIC block.

(*) The MB Cosmic decision is derived by first requiring the coincidence of hits at both ends of the MB readout chambers and then counting all hits in the inner (top plus bottom) and outer (top plus bottom) MB barrel layers. When both inner and outer hit multiplicities are above threshold, the MB Cosmic decision bit is set to 1.

Veto Fiber	Output Bit	Description
Collar (CC04)	CC(0)	Peak sum fibers 0 to 3
Collar (CC04)	CC(1)	Multiplicity sum fibers 0 to 3
Collar (CC03)	CC(4)	Peak sum fibers 4 to 6
Collar (CC03)	CC(5)	Multiplicity sum fibers 4 to 6
Collar (CC05)	CC(8)	Peak sum fibers 8 to 11
Collar (CC05)	CC(9)	Multiplicity sum fibers 8 to 11
Collar (CC06)	CC(12)	Peak sum fibers 12 to 15
Collar (CC06)	CC(13)	Multiplicity sum fibers 12 to 15
BPCV Peak	BPCV(0)	Peak sum BPCV fiber
BHTS1 Peak	BH(0)	Peak fiber 0
BHTS2 Peak	BH(1)	Peak fiber 1
BHCV Peak	BH(2)	Peak sum fiber 2-3
BHGC Peak	BH(3)	Peak sum fiber 4-5
BHCV Coincidence	BH(4)	BHCV Peak .AND. BHTS1 Gate
BHCV Coincidence 2	BH(5)	BHCV Peak .AND. BHTS2 Gate
BHCV Double Coincidence	BH(6)	BHCV Peak .AND. BHTS1 Gate .AND. BHTS2 Gate
new BHCV Total	BH(7)	Peak sum fibers 0 to 16
new BHCV Hit	BH(8)	Summed Multiplicity BHCV1, BHCV2 and BHCV3
BHPV Peak	BH(12)	Peak sum fibers 8 to 15
BHPV Hit	BH(13)	Summed Multiplicity of BHPV1 to BHPV8

Table 5: Description of veto fiber output bits sent from L1 Veto fibers to Master Veto board: for a definition of **peak**, **gate** and **multiplicity**, see caption of Table 4. The Output Bit label reflects the name of the L1 Veto module listed in Table 3. The logic used to generate the Collar and BH triggers is implemented inside the NEW_L1VETO_LOGIC. The logic used for the BPCV trigger is implemented inside the COSMIC_LOGIC block within the NEW_MASTER_VETO block.

(*) Dual hit is the coincidence of hits in adjacent COSMIC MB ADC channels, i.e. in channels (0,1), (2,3)...(14,15).
(**) FB Cosmic coincidence is defined as a 4-fold coincidence of hits in Cosmic CAL ADC channel 0,1,2 and 3.
(***) Top CsI coincidence is defined as the logical OR of hit coincidences for Cosmic CAL ADC channels (4,5), (6,7) and (8,9).
$^{(\circ *)}$ Bottom CsI coincidence is defined as the logical OR of hit coincidences for Cosmic CAL ADC channels (10,11), (12,13) and (14,15).
$^{(\circ)}$ The BHPV pair trigger divides BHPV in 12 equivalent channels by pairing up channels (0,1) and (2,3) from each BHPV ADC, and requires the coincidence over all of the 12 pairs.

4 Control Registers

(a) The "TLK Errors Count" register reports the number of fiber transmission errors, that is the number of 8ns clock samplings for which the the RX_DV and RX_ER outputs of the TLK chip are both high. The "Single-Bit Error Count" reports the number of 8 ns samplings for which the data is different from the ADC generated random sequence. Both counts are only for fiber enables via the 'Set Error Counter Mask' register (0xBC) (see note (j)).

(b) The "TLK Error Position" register reports which input fiber had the last TLK error by driving high the bit corresponding to the input fiber number (that is bit(i)=1 if input fiber i has the TLK error). The "Single-Bit Error Position" register reports which input fiber had the last single bit error by driving high the bit corresponding to the input fiber number plus 16. (that is bit(16+i)=1 if input fiber i has the a single-bit error. Position errors are reported only for fibers previously enabled via the 'Set Error Counter Mask' register (0xBC) (see note (j)).

(c) This register selects to receive either the backplane/front-panel LIVE and L1A by writing 0/1 to bit(0).Its default value is 0, meaning that the backplane signals are used. The status of this signal is monitored via bit(3) of the status register 0xEC. Bit(1/2) of register 0XEC monitor the status of BKPLN_LIVE/FRONT_LIVE. The status of LIVE, independently of the source, is monitored by bit(0).

(d) Total number of L1A seen from the last board reset.

(e) Read number of 8 ns clock cycles from LIVE before a non zero value is seen. Bits(7:0) read the counts for the local energy sum/veto bit data. Bits(23:16) read the count for the input daisy-chain info. In order for these counts to be correct, the "Daisy-Chain Calibration Enable" bit(24) of register 0xCC must be set to 1 (see note (o)).

(f) Simulate the content of the daisy-chain input(output) when bit 16(17) of register 0xCC is set to 0. Default value is zero.

(g) Set the delay for the local sum/veto bit data so that it aligns with the daisy chain inputs. Must be set equal to the difference between the two delays returned by register 0x5C after the delay calibration run (see note (e)).

(h) Set the maximum number of TLK errors allowed in one LIVE. At power up or after a firmware reset, the default value for this register is 0x20. When the number of TLK errors goes over this maximum, bit(7) of Status Register 0xEC goes high until the end of LIVE.

(i) Set the delay between LIVE and ENABLE_SUM. ENABLE_SUM is the signal that enables the data from L1 fiber inputs to get out of the SUM_ALIGNMENT block. At power up or after a board reset, the default value for this register is 0x3C (dec 60). This delay has to be set larger than the value measured by the "Input Delay Calibration" register 0x54 (see note (s)). At the same time, a maximum value of 0x80 (dec 128) is allowed to

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read TLK Error Count$^{(a)}$	16	RO	0xc	data[15:0]
Read Single-bit Error Count$^{(b)}$	16	RO	0xc	data[31:16]
Read TLK Error Position$^{(a)}$	16	RO	0x1c	data[15:0]
Read Single-Bit Error Position$^{(b)}$	16	RO	0x1c	data[31:16]
Select LIVE/L1A source$^{(c)}$	1	WO	0x2c	data[0]
Read L1A Counter$^{(d)}$	16	RO	0x3c	data[15:0]
Counters Reset$^{(z)}$	1	WO	0x4c	data[0]
Daisy-chain Calibration Result$^{(e)}$	16	RO	0x5c	data[23:16,7:0]
Set Input Daisy-chain Energy$^{(f)}$	24	RW	0x6c	data[23:0]
Set Output Daisy-chain Energy$^{(f)}$	24	RW	0x7c	data[23:0]
Set adder-tree delay$^{(g)}$	7	RW	0x8c	data[6:0]
Set max. TLK errror count$^{(h)}$	16	RW	0x9c	data[15:0]
Set Delay for LIVE$^{(i)}$	7	RW	0xac	data[6:0]
Set Error Counter Mask$^{(j)}$	32	RW	0xbc	data[31:0]
Set Enables (see Table 8)	32	RW	0xcc	data[31:0]
FIFO Reset$^{(z)}$	1	WO	0xdc	data[0]
Read Status bits (see Table 9)	32	RO	0xec	data[31:0]
Firmware VME Reset$^{(z)}$	1	WO	0xfc	data[0]
Read Daisy-Chain Single-bit Error$^{(p)}$	32	RO	0x4	data[31:0]
Set Single Crate Thresholds$^{(q)}$	24	RW	0x14	data[23:0]
Set Thresh. for Veto Sum of fibers 0-15$^{(r)}$	20	RW	0x24	data[19:0]
Set Thresh. for Veto Sum of fibers 0-6$^{(r)}$	20	RW	0x34	data[19:0]
Set Thresh. for Veto Sum of fibers 8-15$^{(r)}$	20	RW	0x44	data[19:0]
Read Input Delay Calibration$^{(s)}$	8	RO	0x54	data[7:0]
Set Pedestal Subtraction Energy$^{(t)}$	20	WR	0x64	data[19:0]
Set Thresh. for Veto Sum of fibers 0-3$^{(r)}$	20	RW	0x74	data[19:0]
Set Thresh. for Veto Sum of fibers 4-6$^{(r)}$	20	RW	0x84	data[19:0]
Set Thresh. for Veto Sum of fibers 8-11$^{(r)}$	20	RW	0x94	data[19:0]
Set Thresh. for Veto Sum of fibers 12-15$^{(r)}$	20	RW	0xa4	data[19:0]
Set Thresh. for Veto Multiplicity$^{(u)}$	24	RW	0xb4	data[23:0]
Set Input Delay Enable$^{(n)(v)}$	16	RW	0xc4	data[15:0]
Set Thresh. for Cosmic Veto Multiplicity $^{(u)}$	3x5	RW	0xd4	data[23:0]
Set Thresh. for Veto Multiplicity by 4$^{(u)}$	32	RW	0xf4	data[31:0]

Table 6: List of User Defined Registers defined for the L1 TRIGGER board.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Set BHTS1 Threshold	16	RW	0x100	data[15:0]
Set BHTS2 Threshold	16	RW	0x110	data[15:0]
Set BHCV Threshold	17	RW	0x120	data[16:0]
Set BHGC Threshold	17	RW	0x130	data[16:0]
Set Thresh. for new BHCV Multiplicity	4	RW	0x140	data[3:0]
Set Thresh. for BPHV Multiplicity	2	RW	0x150	data[1:0]
Set BPCV Threshold	15	RW	0x160	data[15:0]
Set BHPV1 Threshold	16	RW	0x180	data[15:0]
Set BHPV2 Threshold	16	RW	0x190	data[15:0]
Set BHPV3 Threshold	16	RW	0x1A0	data[15:0]
Set BHPV4 Threshold	16	RW	0x1B0	data[15:0]
Set BHPV5 Threshold	16	RW	0x1C0	data[15:0]
Set BHPV6 Threshold	16	RW	0x1D0	data[15:0]
Set BHPV7 Threshold	16	RW	0x1E0	data[15:0]
Set BHPV8 Threshold	16	RW	0x1F0	data[15:0]

Table 7: Continuation of User Defined Registers defined for the L1 TRIGGER board.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Set Input Fiber Mask$^{(k)}$	16	RW	0xcc	data[15:0]
Set Daisy-Chain Input Enable$^{(k)}$	1	RW	0xcc	data[16]
Set Daisy-Chain Output Enable$^{(k)}$	1	RW	0xcc	data[17]
Set Single Crate Threshold$^{(l)}$	1	RW	0xcc	data[18]
Set Master Veto board $^{(m)}$	1	RW	0xcc	data[20]
Set Left vs Right Master Veto$^{(m)}$	1	RW	0xcc	data[21]
Set L1Veto board flavor$^{(n)}$	1	RW	0xcc	data[23]
Daisy-Chain Calibration Enable$^{(o)}$	1	RW	0xcc	data[24]
Set CV L1Veto board$^{(n)}$	1	RW	0xcc	data[26]
Set OEV L1Veto board$^{(n)}$	1	RW	0xcc	data[27]
Set NCC L1Veto board$^{(n)}$	1	RW	0xcc	data[28]
Set MB_FB L1Veto board$^{(n)}$	1	RW	0xcc	data[29]
Set BH L1Veto board$^{(n)}$	1	RW	0xcc	data[30]
Set COLLAR L1Veto board$^{(n)}$	1	RW	0xcc	data[31]

Table 8: List of board enables and masks defined via register 0xCC. At power up or after a board reset, the default value is 0x3FFFF.

Status of LIVE$^{(c)}$	1	RO	0xec	data[0]
Status of Bkpln LIVE$^{(c)}$	1	RO	0xec	data[1]
Status of Front panel Live$^{(c)}$	1	RO	0xec	data[2]
Status of LIVE/L1A Source Select$^{(c)}$	1	RO	0xec	data[3]
Status of Input FIFOs Full Line$^{(w)}$	1	RO	0xec	data[4]
Status of K0TO_ERROR Signal$^{(x)}$	1	RO	0xec	data[5]
Status of Internal Energy Sum Ovfl.$^{(t)}$	1	RO	0xec	data[6]
Status of TLK Error Counter$^{(h)}$	1	RO	0xec	data[7]
Board Revision$^{(y)}$	4	RO	0xec	data[19:16]
Firmware Revision$^{(y)}$	4	RO	0xec	data[23:20]
Firmware Version$^{(y)}$	4	RO	0xec	data[27:24]
Board Type$^{(y)}$	4	RO	0xec	data[31:28]

Table 9: Content of Status Register bits for the L1 TRIGGER Board.

prevent the FIFO inside the the "sum_alignment" block from overflowing. It will reset itself automatically to the default value if a value greater than 0x80 is downloaded.

(j) Bit(i) (i=0 thru 15) are used to enable data from the *i-th* input fiber into the TLK/Single-bit Error counter logic. Bit(j+16) (j=0 thru 15) are used to select which of the *j-th* input fiber are connected to the previous board in the daisy chain (see note (p)). At power up or after a board reset, the default value for these bits is all 0.

(k) Bit(i) (i=0 thru 15) are used to enable data from the *i-th* input fiber inside the firmware. Bit(16/17) is used to enable the input/output daisy-chain data into/out of the firmware. The default value for all these bits is 1.

(l) When this bit is low (default), the total calorimeter energy is passed to the P3 daisy chain for the L1 Trigger decision. When this bit is high, the local energy sum is compared to a local threshold, set by register 0x14 (see note (q)), and the resulting ADC crate trigger decision (CSUM or Regional Trigger) is passed to the P3 daisy chain. For the May 2013 run, a separate path was used to pass the Regional Trigger to Master MACTRIS so that both the total CsI energy and the CSUM info from all of the CsI L1 boards could be used in the final L1A decision. A CSUM trigger was generated at the peak of the local energy sum above threshold and passed as a pulse 3-clk cycles long to the K0TO_PTP1 P3 backplane signal.

(m) When bit(20) of register 0xCC is high, the Master Veto flavor of the L1 Trigger board firmware is selected and daisy-chain bits (23:18) are driven to the daisy-chain output, together with bits (17:0) for the sum of the eight CsI input fibers connected to the Master Veto board. When bit(20) is low (default), the CsI calorimeter flavor of the L1 Trigger board is selected. In this case, bits(23:18) of the input daisy chain are passed to the output daisy chain unchanged, while the local energy sum is added to the input daisy chain energy and passed along the output daisy chain. Together with this "Set Master Veto Board", the

"Set Left vs Right Master Veto" bit(21) of register 0xCC has to set high for the Master Veto board in slot 4 and low (default) for the Master Veto boards in slot 20. This determines the mapping between input L1 veto fibers and bits (23:18) in the P3 backplane (see Table 3 for details).

(n) When bit(23) of register 0xCC is high, the L1 Veto flavor of the L1 Trigger board firmware is selected (default is 0, i.e. the CsI L1 Trigger board firmware). Bits(31:24) of register 0xCC further select which sets of 16 veto decisions generated inside the NEW_L1VETO_LOGIC block are to be driven out of the input 7 fiber. This depends on the position of the L1 Veto board in the crate (see Table 2). The specific veto decision, that is which of the 16 bits passed by a fiber is to be enabled onto the L1 Veto fiber all the way to Master Veto, is selected by bit(31:16) of register 0xC4. When bit(j+15) (j=0 thru 15) is equal 1 means, the j-th veto decision is enabled. The default for all bits of register 0xC4 is 0.

(o) Bit(24) of register 0xCC must be set high to correctly measure the daisy chain delay. In this condition, the time for LIVE to propagate thru the system is measured by calculating how long it takes to observe the input fiber alignment word, 0xFEFE, at different points inside the firmware. After these delays are calibrated, we must set bit(24) low. This masks out the alignment word before it enters the Energy Adder, or the L1 Veto block, and avoids spurious triggers.

(p) These register is used when doing stand-alone L1 Trigger board tests or when testing the integrity of the daisy-chain in P3 backplane. The "Daisy-Chain Single-bit Error" reports the number of 8 ns samplings for which the data generated by the local energy sum logic does not agree with the sum of ADC generated random sequence data connected to the adder tree inputs. Bit(15:0) report errors for the output of the single board adder tree while bit(31:16) report for the comparison of the input daisy-chain. The test takes automatically into account the number of fibers enabled into the L1 firmware (using bit(15:0) of register 0xCC) and the number of fibers enabled in the L1 Trigger boards feeding the data to the input daisy-chain (using bit(31:16) of register 0xBC).

(q) This register sets the local threshold used for the crate sum trigger, or regional trigger, decision. To switch from sending the total calorimeter energy sum to the number of regional trigger via the daisy-chain to Master MACTRIS, bit(18) of register 0xCC must be set high. The default for the threshold is 0.

(r) These registers set the thresholds for the partial energy sums used in the L1Veto logic. The default for all of these registers is 0xFFFFFF.

(s) This register reports the delay between LIVE and the capture of the 0xFEFE alignment word by all of the input fibers specified by the "Set Fiber to Adder Enables" register (0xCC). This is a measure of the maximum delay between LIVE being generated by MACTRIS and ADC energies being received by the L1 Trigger board. It determines the minimum value allowed for the "Set Delay for LIVE" register (0xAC) during physics data. Note that in order for this delay to be properly measured, the "Daisy Chain Calibration Enable"

(bit(24)) of register 0xCC has to be set to 1 and the delay of ENABLE_SUM itself has to be set to its maximum value via register 0xAC (see note (i).

(t) This register set the energy to be subtracted for the internal energy sum generated by the ENERGY_ADDER block. It prevents the energy sum from overflowing the allocated 18 bits in the P3 daisy-chain when no pedestal subtraction is done in the ADCs. A reading of the raw internal energy sum can be done via the energy monitoring register 0xB8. The pedestal subtraction is disabled when the board is in "calibration" mode. The OR of the pedestal subtracted energy bit(19:16) is monitored via bit(6) of the Status register 0xec.

(u) These registers set the thresholds for the counter of veto hit multiplicity used in the L1Veto logic. Bit(7:0) of register 0xB4 set the thresholds for sum over input fibers 0 to 15, bit(15:8) for the sum over input fibers 0 to 6 and bit(23:16) for the sum over input fibers 8 to 15. Bit(7:0) of register 0xF4 set the thresholds for sum over input fibers 0 to 3, bit(15:8) for the sum over input fibers 4 to 6, bit(23:16) for the sum over input fibers 8 to 11 and bit(31:24) for the sum over input fibers 12 to 15.. Finally, bit(4:0) of register 0xD4 set the thresholds for the hit multiplicity in the Inner MB, bit(12:8) in the Outer MB and bit(27:24) for the MB Cosmic decision (for a description, see Table 4). The default for all of these bits is 1.

(v) Bit(i) (i=0 thru 15) is used to enable an extra 16 nsec delay at the output of the SUM_ALIGNMENT block for the i-th fiber. This delay is needed for fibers reading out small CsI crystal when mixed with fibers reading out large CsI crystals, since the response of the large CsI crystals is slower by about 16 ns. When bit(i) is set to zero, input fiber i will add two 8-ns sampling of zero energies to the output of the fiber alignment block. When bit(i) is set to 1, no extra delay is added to the input fiber energy. Bit(j+15) (j=0 thru 15) is used to mask the j-th veto bit from coming out of the L1Veto board fiber 7 output (see note (n)). At power up or after a board reset, the default value for all bits of register 0xC4 is 1.

(w) This signal monitors the OR of the FULL outputs for all of the FIFOs inside the SUM_ALIGNMENT block.

(x) This signal is high when any TLK error from an enabled input fiber is detected.

(y) The MSB 16 bits of register 0xec carry information about the board and firmware, namely bit(19:16) encode a unique value for the TRIGGER board hardware version type (0x0 for old Trigger board, 0xB for revB board, 0xC for revC TRIGGER board); bit(23:20) and bit(27:24) encode the firmare version and revision number; but(31:28) encode a unique value for each trigger board in the system (0x1 for L1 Trigger, 0x2 for L2 Trigger, 0x4 for MACTRIS)

(z) By writing 1 to bit(0) of these registers we reset different parts of the firmware. More specifically, 0x4c resets all of the counters to zero, 0xdc clears the contents of the FIFOs and 0xfc resets all of the VME controlled registers to their default value.

5 Energy Diagnostic Registers

The L1 TRIGGER firmware has multiple registers designed to capture the energy of the incoming fibers as well as the progression of the energy sum inside the firmware. They are listed in Tables 10 and 11, respectively.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read fiber 0	32	RO	0x0	data[31:0]
Read fiber 1	32	RO	0x10	data[31:0]
Read fiber 2	32	RO	0x20	data[31:0]
Read fiber 3	32	RO	0x30	data[31:0]
Read fiber 4	32	RO	0x40	data[31:0]
Read fiber 5	32	RO	0x50	data[31:0]
Read fiber 6	32	RO	0x60	data[31:0]
Read fiber 7	32	RO	0x70	data[31:0]
Read fiber 8	32	RO	0x80	data[31:0]
Read fiber 9	32	RO	0x90	data[31:0]
Read fiber 10	32	RO	0xa0	data[31:0]
Read fiber 11	32	RO	0xb0	data[31:0]
Read fiber 12	32	RO	0xc0	data[31:0]
Read fiber 13	32	RO	0xd0	data[31:0]
Read fiber 14	32	RO	0xe0	data[31:0]
Read fiber 15	32	RO	0xf0	data[31:0]

Table 10: List of the single fiber energy monitoring registers.

The 31 bit of data read out for each fiber as per Table 10 contain the following info:

- bits (31:16) are the energy data readout at the input of each fiber, ie the energies generate by the TLK receiver outputs registered by that specific TLK recovered clock. When LIVE is low, they will read the IDLE word 0x50BC.
- bits (15:0) are the energy data for each fiber after being aligned with the 8 ns master clock. These are also the inputs to the ENERGY_ADDER, NEW_L1VETO_LOGIC or NEW_MASTER_VETO blocks. When LIVE is low, they will read zero. When LIVE is high, they will have non zero reading only when they are enabled by the relevant bit in the "Input Fiber Mask" of register 0xCC.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read sum fibers 0 thru 3	18	RO	0x8	data[17:0]
Read sum fibers 4 thru 7	18	RO	0x18	data[17:0]
Read sum fibers 9 thru 12	18	RO	0x28	data[17:0]
Read sum fibers 13 thru 15	18	RO	0x38	data[17:0]
Read sum fibers 0 thru 7	19	RO	0x48	data[18:0]
Read sum fibers 8 thru 15	19	RO	0x58	data[18:0]
Read sum hits MB inner	5	RO	0x78	data[4:0]
Read sum hits MB outer	5	RO	0x88	data[4:0]
Read raw sum fibers 0 thru 15	20	RO	0xb8	data[19:0]
Read daisy-chain input 24 bits	24	RO	0xc8	data[23:0]
Read sum energy and L1 veto bits	24	RO	0xd8	data[23:0]
Read sum of internal & daisy-chain bits	24	RO	0xe8	data[23:0]
Read daisy-chain output 24 bits	24	RO	0xf8	data[23:0]

Table 11: List of the registers monitoring the total energy at various points inside the firmware and MB hit multiplicity. Sum fibers are at the exit of the ENERGY_ADDER block, before pedestal subtraction.

6 Schematics Description

Sheet 1 Input and Output Clock logic; Heart-bit and VME Activity LED Logic. Reset logic.

Sheet 2 VME Interface; Firmware Version bits. VME commands definition.

Sheet 3 LIVE and L1A Control Logic; LIVE Delay Logic and L1A Counter.

Sheet 4 TLK Mask and Error Counter Logic. VME read-only registers definition.

Sheet 5 Fiber Alignment Logic with SUM_ALIGNMENT blocks.

Sheet 6 Fiber Enable to Adder Tree and Veto Logic

Sheet 7 Input Energy Diagnostic fibers 0 thru 7

Sheet 8 Input Energy Diagnostic fibers 8 thru 15

Sheet 9 Adder Tree Logic and Local Energy Sum Logic. CRATE SUM decision logic.

Sheet 10 Daisy-Chain Delay Calibration Logic and Input Fiber Alignment Calibration Logic

Sheet 11 Partial Energy Sum and Veto Bit Counters Diagnostic Logic.

Sheet 12 Random Sequence Generator; Single-bit Error Counters.

Sheet 13 Single-bit Error Detection Logic.

Sheet 14 Adder Tree Single-bit Error Detection Logic

Sheet 15 Daisy-chain Single-bit Error Detection Logic

Sheet 16 VME R/W Registers Definition. CRATE SUM peak trigger logic and shaping. Input Veto and CSUM triggers delay Logic.

Sheet 17 L1Veto fiber Alignment Logic. TLK control signals definition.

Sheet 18 NEW_MASTER_VETO block and veto bits P3 drivers.

Sheet 19 Single fiber hits adders.

Sheet 20 NEW_L1VETO_LOGIC and MB_COSMIC_LOGIC blocks.

Sheet 21 VME Registers for veto bit thresholds.

Sheet 22 VME Registers for BHCV/BHPV/BPCV veto thresholds.

Sheet 23 Firmware Versioning History