KOTO Note XXX
Version 3.0
February 14, 2017

L1 TRIGGER Board VME Address Space for June 2016 Run

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This document specifies the VME Address Space defined in the firmware of the L1 TRIGGER board. The L1 TRIGGER board is designed to receive data from up to 16 L1 fibers carrying the sum of the energy over the sixteen analog inputs serviced by a single ADC board. The fiber data is deserialized in external SERDES chips before reaching the firmware, where it is aligned to the start of the LIVE gate, summed together and sent out to a 24-bit daisy-chain bus. For run 69 (May-June 2016), all of the trigger boards in the L1 Trigger crate were downloaded with version v5.5 of the Virtex5 firmware (the same used for run 62 thru 65) while the two boards in the new L1 Veto crate were downloaded with version v5.8. Both versions of the firmware were designed to interface with the new Master Control (MACTRIS+) board.

1 Introduction

The L1 TRIGGER board is the rev-C2 revision of a 9U VME module designed to receive data from up to 16 fibers running at 2.5Gb/s connected to its input port 0 thru 15, deserialize the fiber data via Texas Instruments TLK3101 transceivers and send the parallel 16-bits of recovered data every 8-ns to an on board Virtex 5 Xilinx FPGA (XC5VFX70T) [1]. It can also transmit signals out of the fiber connected to input port 7. The same board design is used in both the L1 Trigger and the L2 Trigger crates, the only difference being the version of the firmware downloaded to the board and the ADC fiber connected to its input ports. The L1 TRIGGER board receives data from the L1 fiber (second fiber from the top of the ADC board front panel) while the L2 TRIGGER board receive data from the fL2 fiber (first fiber from the top).

There are 3 flavors of L1 TRIGGER boards, selectable via programmable switches in the firmware: **L1TRG** boards, which receive energy sums from up to 16 ADCs connected to the CsI calorimeter; **L1Veto** boards, which receive energy sums or hit multiplicities from up to 15 ADCs connected to one or more veto detectors and is able to drive veto trigger decision via the port 7 fiber; and **Master Veto** boards, which receive 8 fibers of energy sums from CsI ADCs and 8 fibers of veto trigger decision from L1Veto boards. Different flavor of boards can

[1] The trigger board houses a second Xilinx FPGA (XC4VFX12) which is not functionally used in the L1 TRIGGER logic but has to be downloaded with either v1.0 or v1.1 of the dummy "L1Trigger_Virtex4" design

be installed only in specific predefined slots in the crate as they drive different signals to the P3 backplane.

In the following, section 2 gives an overview of the configuration of the L1 Trigger and L1 Veto crates. Section 3 contains a description of the main hardware and firmware features of the L1 TRIGGER board. The remaining sections list the registers defined inside the FPGA to simulate and control the different board functionalities: section 4 reports on miscellaneous command and control registers; section 5 reports on the registers used to monitor the incoming fiber energies and the internal energy sums. Finally section 6 lists the content of the current versions of the "L1Trigger_Virtex5" firmware (mostly in ISE schematics entry) sheet-by-sheet.

2 The L1 Trigger and L1 Veto Crates

The **L1 Trigger** crate is a 21-slot 9U VME64x crate with a modified P2 backplane and a custom-made P3 backplane. Similarly, the **L1 Veto** crate is a 9U VME64x crate added in the June 2016 run to the NIM rack adjacent to the Trigger rack in Hadron Hall. Both use the P2 backplane to distribute VME signals and special DAQ Control signals to all boards in the crate. The DAQ controls comprise two sets of differential lines used to carry the 125 MHz system clock and the L1A trigger decision, plus multiple single ended bussed lines described in Table 1. Most of the single ended lines are negative logic Low Voltage TTL (LVTTL) signals but some are Open Collector (OC). The first are used to carry information from MACTRIS+ to the L1 TRIGGER boards while the second communicate information back to MACTRIS+. In the present DAQ architecture, the Master MACTRIS board is located in slot 12 of the L1 Trigger crate and can distribute a copy of the DAQ Controls to up to four individual crates via by a Slave MACTRIS board located in slot 2.

The P3 backplane is a custom backplane designed to connect specific slots in the crate via daisy-chain. There are two daisy-chains, the left and the right, originating in slot 4 and 20 and ending in slot 12. On the way to slot 12, they connect together only slots 4-5-6-9-10-11 and 20-19-18-15-14-13, respectively. Each daisy-chain comprises a 24 bit bus, with bit(17:0) reserved for energy signals and bit(23:18) for veto signals.

In the L1 Trigger crate, five of the slots in each daisy-chain are reserved for L1TRG boards, which service most of the 2708 crystals comprising the CsI calorimeter. The two outermost daisy-chain slots (4 and 20) are occupied by the left and right Master Veto boards, which are programmed to receive both CsI fibers at inputs port 8 to 15 and L1Veto fibers at input ports 0 to 7. The remaining available slots in the crate (3, 7, 8, 16, 17 and 21) are used by L1Veto boards. The L1 Veto crate added for the June 2016 run services two L1Veto boards in slot 8 and 16, each receiving signals from 8 Inner Barrel (IB) ADC boards via input ports 8 to 15. The L1Veto boards are able to generate up to 16 independent veto triggers based on the comparison of total and partial energy sums or hit multiplicities to programmable thresholds. Table 2 and Figure 1 summarize the location, input fiber origin and port connection for all the boards in the L1 Trigger and L1 Veto crates.

For the June 2016 run, all ADC boards were 125 MHz except for the boards digitizing the beam hole veto detectors (BHPV and BHCV) and the Inner Barrel (IB) detector, which are 500 MHz boards with 4 analog input each. For the 125 MHz boards, hit multiplicity is

DAQ Signal	Pin	Level	DAQ Signal	Pin	Level
CLK+	A6	diff. PECL	L1A_EN	C2	LVTTL
CLK-	A7	diff. PECL	L1A+	C4	diff. PECL
BEAM_ON	A9	LVTTL	L1A-	C5	diff. PECL
SPILL_ON	A10	LVTTL	LIVE	C12	LVTTL
L2A	A12	LVTTL	LIVE_EN	C13	LVTTL
L2A_EN	A13	LVTTL	K0TO_HOLD	C16	LVTTL
K0TO_RESET	A15	LVTTL	K0TO_RUN	C17	LVTTL
K0TO_HALT	A16	LVTTL	L2B(0)	C20	LVTTL
K0TO_RECOVER	A18	LVTTL	L2B(1)	C21	LVTTL
K0TO_SAVE	A20	LVTTL	L2B(2)	C22	LVTTL
K0TO_READ	A21	LVTTL	L2B(3)	C23	LVTTL
K0TO_NOT_EMPTY	A23	OC	L2B(4)	C24	LVTTL
K0TO_FULL	A24	OC	L2B(5)	C25	LVTTL
K0TO_ERROR	A26	OC	RDB(0)	C27	LVTTL
K0TO_DONE	A27	OC	RDB(1)	C28	LVTTL
K0TO_OC_RSVD	A30	OC	RDB(2)	C29	LVTTL
K0TO_RSVD	A31	LVTTL	RDB(3)	C30	LVTTL
			RDB(4)	C31	LVTTL
			RDB(5)	C32	LVTTL

Table 1: List of DAQ Control Signals and their mapping in the P2 backplane pins. The "Level" column specify their electrical logic level: LVTTL and differential PECL signals are generated by MACTRIS+ and received by the L1 TRIGGER boards; Open Collector (OC) signals are driven by any of the L1 TRIGGER boards and received by MACTRIS+. All of the signals are negative logic. In the present L1 TRIGGER board firmware, only CLK, L1A, LIVE and K0TO_ERROR are used. The last is used to indicate that a large number of TLK errors is observed for that board (see note (h) in section 4).

simply defined as the sum over any of the 16 ADC channels found to have energy above a predefined threshold in any given 8-ns sample. For the 500 MHz boards, hits from the four ADC channels are multiplexed into the 16-bit of data carried by a L1 fiber according to the following scheme (h_{00},h_{10}, h_{20},h_{30},h_{01},h_{11}...h_{23},h_{33}), where h_{xy} is the hit in the xth channel for the yth 2-ns sampling. Hit multiplicity in a given 8-ns sampling is then defined as the logical OR of the four 2-ns hits from the same channel, that is channel 0 hit multiplicity is calculated as (h_{00}.OR. h_{01}.OR.h_{02}.OR.h_{03}).

L1 Trigger Slot	L1 Trigger board flavor	Fiber Origin	Input Port Usage
3	Front CV L1Veto	A11-3/5, A116/8	0-2, 4-6
3	Rear CV L1Veto	A11-9/11,A11-12/14	8-10, 12-14
4	Left Master L1Veto	(see Table 3)	0-7
4	Left Master L1Veto	A5-3 to A5-10	8-15
5	Csi L1TRG	A4-3 to A4-18	0-15
6	Csi L1TRG	A3-3 to A3-18	0-15
7	Up/Downstream BCV L1Veto	A14-7/8, A14-13/14	0-3
7	FB Veto	A13-16/17	4-5
7	Up/Downstream Inner MB L1Veto	A14-3/4, A14-9/10	8-11
7	Up/Downstream Outer MB L1Veto	A14-5/6, A14-11/12	12-15
8	Common NCC L1 Veto	A13-3 to A13-6	0-3
8	Front NCC L1Veto	A13-7 to A13- 9	4-6
8	Middle NCC L1Veto	A13-10 to A13-12	8-10
8	Rear NCC L1Veto	A13-13 to A13-15	12-14
9	Csi L1TRG	A2-3 to A2-18	0-15
10	Csi L1TRG	A1-3 to A1-18	0-15
11	Csi L1TRG	A0-3 to A0-18	0-15
13	Csi L1TRG	A10-3 to A10-18	0-15
14	Csi L1TRG	A9-3 to A9-18	0-15
15	Csi L1TRG	A8-3 to A8-18	0-15
16	OEV L1Veto	A11-16 to A11-18	0-2
17	new BHCV1 L1Veto(*)	A16-3 to A16-6	0-3
17	new BHCV2 L1Veto(*)	A16-7 to A16-10	7-11
17	new BHCV3 L1Veto(*)	A16-11 to A16-14	12-15
18	Csi L1TRG	A7-3 to A7-18	0-15
19	Csi L1TRG	A6-3 to A6-18	0-15
20	Right Master Veto	(see Table 3)	0-7
20	Right Master Veto	A5-11 to A5-18	8-15
21	CC04 Collar L1 Veto	A12-5 to A12-8	0-3
21	CCO3 Collar L1 Veto	A12-3/4	4-5
21	CCO5 Collar L1 Veto	A12-13 to A12-16	8-11
21	CCO6 Collar L1 Veto	A12-9 to A12-12	12-15
L1 Veto slot			
8	Upstream IB L1Veto(*)	A17-3 to A17-10	8-15
16	Downstream IB L1Veto(*)	A17-11 to A17-18	8-15

Table 2: L1 TRIGGER board slot position and board flavor in the L1 Trigger and L1 Veto crates. The Fiber Origin indicates which ADC board drives the L1 fiber as ADC crate number-slot number. The Input Port Usage specify which of the L1 TRIGGER input ports are used. (*) These L1Veto boards are connected to 500 MHz ADC boards.

fiber_map

L1TRG INPUT TO ADC LOCATION MAPPING: AiCj means fiber from slot j of ADC crate i

Detector	CV	LEFT Master CsI	Csi	CsI	FB/ MB	NCC	Csi	Csi	CsI		CsI	CsI	CsI	OEV	BHCV/BHPV	CsI	CsI	Right Master CsI	CCOX	Veto Crate Upstream IB	Veto Crate Downstream IB
L1 slot	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**8**	**16**
input 0	A11-03	L1Veto-1	A4-03	A3-03	A14-07	A13-3	A2-03	A1-03	A0-03		A10-03	A9-03	A8-03	A11-16	A16-03	A7-03	A6-03	L1Veto-6	A12-05		
input 1	A11-04	L1Veto-2	A4-04	A3-04	A14-08	A13-4	A2-04	A1-04	A0-04		A10-04	A9-04	A8-04	A11-17	A16-04	A7-04	A6-04	L1Veto-5	A12-06		
input 2	A11-05	L1Veto-3	A4-05	A3-05	A14-13	A13-5	A2-05	A1-05	A0-05		A10-05	A9-05	A8-05	A11-18	A16-05	A7-05	A6-05		A12-07		
input 3		L1Veto-4	A4-06	A3-06	A14-14	A13-06	A2-06	A1-06	A0-06		A10-06	A9-06	A8-06		A16-06	A7-06	A6-06		A12-08		
input 4	A11-06	L1Veto-7	A4-07	A3-07	A13-16	A13-07	A2-07	A1-07	A0-07		A10-07	A9-07	A8-07			A7-07	A6-07		A12-03		
input 5	A11-07	L1Veto-8	A4-08	A3-08	A13-17	A13-08	A2-08	A1-08	A0-08		A10-08	A9-08	A8-08			A7-08	A6-08		A12-04		
input 6	A11-08	A14-18(*)	A4-09	A3-09		A13-09	A2-09	A1-09	A0-09		A10-09	A9-09	A8-09			A7-09	A6-09				
input 7	L1Veto-1	A11-15	A4-10	A3-10	L1Veto-F2	L1Veto-3	A2-10	A1-10	A0-10		A10-10	A9-10	A8-10	L1Veto-4	L1Veto-5	A7-10	A6-10		L1Veto-6	L1-Veto 7	L1Veto 8
input 8	A11-09	A5-03	A4-11	A3-11	A14-03	A13-10	A2-11	A1-11	A0-11		A10-11	A9-11	A8-11		A16-07	A7-11	A6-11	A5-11	A12-13	A17-3	A17-11
input 9	A11-10	A5-04	A4-12	A3-12	A14-04	A13-11	A2-12	A1-12	A0-12		A10-12	A9-12	A8-12		A16-08	A7-12	A6-12	A5-12	A12-14	A17-4	A17-12
input 10	A11-11	A5-05	A4-13	A3-13	A14-09	A13-12	A2-13	A1-13	A0-13		A10-13	A9-13	A8-13		A16-09	A7-13	A6-13	A5-13	A12-15	A17-5	A17-13
input 11		A5-06	A4-14	A3-14	A14-10		A2-14	A1-14	A0-14		A10-14	A9-14	A8-14		A16-10	A7-14	A6-14	A5-14	A12-16	A17-6	A17-14
input 12	A11-12	A5-07	A4-15	A3-15	A14-05	A13-13	A2-15	A1-15	A0-15		A10-15	A9-15	A8-15		A16-11	A7-15	A6-15	A5-15	A12-09	A17-7	A17-15
input 13	A11-13	A5-08	A4-16	A3-16	A14-06	A13-14	A2-16	A1-16	A0-16		A10-16	A9-16	A8-16		A16-12	A7-16	A6-16	A5-16	A12-10	A17-8	A17-16
input 14	A11-14	A5-09	A4-17	A3-17	A14-11	A13-15	A2-17	A1-17	A0-17		A10-17	A9-17	A8-17		A16-13	A7-17	A6-17	A5-17	A12-11	A17-9	A17-17
input 15		A5-10	A4-18	A3-18	A14-12		A2-18	A1-18	A0-18		A10-18	A9-18	A8-18		A16-14	A7-18	A6-18	A5-18	A12-12	A17-10	A17-18

(*) unused

Figure 1: Diagram of L1 fiber connections for Run 69: L1 TRIGGER input ports from 0 to 15 are on the vertical axis; "Axx-yy" means that the input port is connected to the L1 fiber from ADC board in crate Axx slot yy. "L1Veto-z" are the output fibers from the L1Veto boards, which are connected to ports 0 to 7 of the left and right Master Veto boards.

3 The L1 Trigger Board and its firmware

The Trigger board, see Figure 2, is a 9U VME board with connections to the P1,P0,P2 and P3 backplanes. The front panel receives sixteen 2.5Gbs fibers via Avago optical receivers installed in input ports IN0 to IN15. The fiber data is deserialized in the TLK3101 transceivers and sent to the Virtex 5 FPGA. The Virtex 4 FPGA is connected to the Virtex 5 via a 32-bit data, 5-bit address and 8-bit controls bus (V2V bus). The Virtex 4 controls the communication with the two on-board DDR2 2Gb memories and with the Ethernet PHY. A 1Gb Ethernet port (ETH1) and a RJ45 connector (CTRL) complete the list of available I/Os in the hardware.

For the purpose of processing data for the L1A Trigger decision, there is no need to store data in the 2Gb memories nor to read out data via the 1Gb Ethernet port; hence the Virtex 4 FPGA is not used in the L1 TRIGGER board. The Virtex5 has two main global input clocks: CLK125_OSC, connected to a 125 MHz on-board oscillator; and CLK125_IN, connected to the 8-ns system clock. The system clock can be driven either via the P2 backplane or the CTRL front panel connector by removing/installing a jumper on JP17. In the present DAQ architecture, the backplane clock is used [2].

For firmware v3.8 and above, CLK125_OSC is routed to the CLK125_OUT0 output clock pin via a fast buffer with 24 mA current drive. This output pin in turn drives the master clock input of each TLK3101 chip. Note how driving the TLK3101 chips with the system clock created TLK errors due to sporadic or permanent loss of synchronization for the data received from the ADC fibers [3]. The CLK125_IN clock is fed into a Phase Lock Loop (PLL) and a

[2]The front panel clock can be chosen by setting bit(0) of the 0x2C VME register, as specified in Table 6.

[3]TLK error were probably due to the high jitter of the clock coming into the board via the P3 backplane. The quality of the cables used in the propagation of the system clock to the ADC board through the Fanout boards was also affecting the TLK error. Any cable in the KOTO DAQ used for the system clock transmission, especially the 20ft cable between MACTRIS and Master Fanout, must be a CAT6A Ethernet cable.

Veto detector	Input Port	Input Fiber Bits	P3 backplane Bit
CV	L0	(2:0)	L(18)
MB	L1	(4:0)	L(21)
FB	L1	(14:12)	L(19)
NCC	L2	(15:0)	L(20)
OEV	L3	(1:0)	L(22)
IB Upstream	L4	partial energy sum	L(23)
IB Downstream	L5	partial energy sum	L(23)
LCV (A11-15)	L7	energy sum	L(23)(*)
Collar CC03	R-0	(5:4)	R(18)
Collar CC04	R-0	(1:0)	R(19)
Collar CC05	R-0	(9:8)	R(20)
Collar CC06	R-0	(13:12)	R(21)
new BHCV	R-1	(8:7)	R(22)

Table 3: Mapping of veto detectors to Master Veto input ports and P3 backplane bits: the map of veto detectors to L1Veto boards is shown in Table 2, except for the LCV detector which comes directly from the ADC in crate A11 slot 15. The Input Port column shows which of the left(L) or right(R) Master Veto input ports are assigned to a given veto. The Input Fiber Bits column lists the range of independent veto trigger bits, out of the 16 bit of data carried by the fiber, which is driven by a given veto detector. For a veto trigger bit definition, see tables 4 and 5. For IB and LCV, the fiber carries the partial or total energy sum over the whole veto detector. Finally, the P3 Backplane Bit column list which among the left (L) and right (R) daisy-chain bus bits is reserved for the given veto detector. For IB and LCV, the P3 Backplane Bit is set to 1 for the maximum energy sampling above threshold. (*) For Run 69, LCV can drive L(23) if bit(3) of VME register 0x2C is set high; the default value for this bit is zero, meaning that L(23) carries the IB veto trigger.

Digital Clock Manager (DCM) modules instantiated inside the Virtex 5 fabric to generate a zero-delay version of 8-ns system clock used by the rest of the firmware. This clock is routed to the CLK125_OUT1 output clock pin via a fast 24 mA current drive buffer, before it is fanned out to the external registered transceivers used to drive the daisy-chain bus signals to the P3 backplane and the DAQ Controls to the P2 backplane.

The L1 TRIGGER Virtex5 firmware connects the data from the input fibers to different internal logic blocks. The SUM_ALIGNMENT block is responsible for aligning the 16-bit of data recovered from each TLK chip every 8-ns to the system clock and to a common starting time defined by the LIVE gate. The 16-bit input from each fiber is written to a 128-deep FIFO on the edge of the recovered clock when the first sampling of the 0xFEFE alignment word[4] is seen. A delayed version of LIVE called ENABLE_SUM (see note (i) in Section 4) is used to read out simultaneously all of the FIFOs on the 8-ns system clock. The alignment word is

[4]The 0xFEFE word is the first 16-bit word sent from the ADC after LIVE is received. It signals that the active transmission of digitized data via the fiber link has started.

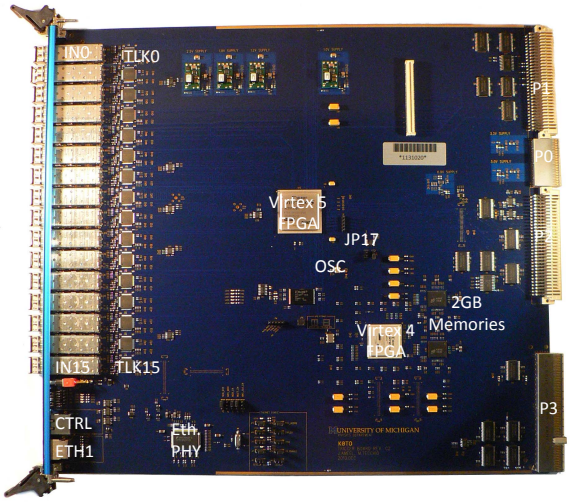

Figure 2: Picture of the TRIGGER board showing the most relevant hardware features.

also used to calibrate the daisy-chain delay by measuring the time delay from the first non-null word at the daisy-chain output driver to the first non-null word seen at the daisy-chain input buffer[5].

Other firmware logic blocks are unique to a certain flavor of L1 TRIGGER board and selectable via VME programmable enables (see Table 7). For the CsI **L1TRG** boards a user-programmable number of fibers is connected to the 4-clk latency ENERGY_ADDER block, where the total energy is calculated and passed to bit(17:0) of the P3 backplane daisy-chain; for the **L1Veto** boards, partial energy and hit multiplicity sums are connected to the 8-clk latency NEW_L1VETO_LOGIC block where up to sixteen independent veto trigger bits per detector are generated (see Tables 4 and 5). These veto bits can be independently enabled before being driven out of the port 7 fiber. The L1Veto output fiber is connected to a predefined input of the Left or Right Master Veto boards as specified in Table 3; for the **Master Veto** boards, input fibers 0 to 7 are connected to a 5-clk latency NEW_MASTER_VETO block, where a single trigger decision per veto detector is calculated as the logical OR of all enabled veto bits and passed to bit(23:18) of the daisy-chain. To correct for the latency of the different logical blocks, extra delays between energy and veto bits are applied by MACTRIS+ before making the final L1 trigger decision.

The Virtex 5 firmware provides also multiple diagnostic and programmable features via VME registers to allow, among other things, the disabling of input ports without a connected fiber, the enabling of extra delay between the input energies, and the monitoring of TLK errors and single-bit errors. In particular, the firmware implements the same 14-bit random sequence which is generated inside the ADC firmware so that a bit-by-bit check of the input fiber energy can be performed at different locations through the firmware. Details on the VME registers used to enable and control all of these features is the subject of the next two sections.

[5]In order to ensure a correct time delay calculation, the board has to be set in a special "calibration mode" which, unlike in normal running conditions, does not mask the alignment word (see note (e) in section 4).

Veto Trigger	Output Bit	Description
Total CV	L0(0)	Peak fibers 0 to 15 sum
Front CV	L0(1)	Peak fibers 0 to 6 sum
Rear CV	L0(2)	Peak fibers 8 to 15 sum
Inner MB	L1(0)	Peak fibers 8 to 11 sum
Outer MB	L1(1)	Peak fibers 12 to 15 sum
Total MB	L1(2)	Peak fibers 8 to 15 sum
BCV	L1(3)	Peak fibers 0 to 3 sum
MB Cosmic	L1(4)	MB Cosmic decision*
FB Energy	L1(12)	Peak fibers 4 to 5 sum
FB Gate	L1(13)	Gate fibers 4 to 5 sum
FB Hits	L1(14)	Multiplicity fibers 4 to 5 sum
Total NCC	L2(0)	Peak fibers 0 to 15 sum
Common+Front NCC	L2(1)	Peak fibers 0 to 6 sum
Middle+Rear NCC	L2(2)	Peak fibers 8 to 15 sum
Common NCC	L2(4)	Peak fibers 0 to 3 sum
Front NCC	L2(5)	Peak fibers 4 to 6 sum
Middle NCC	L2(6)	Peak fibers 8 to 11 sum
Rear NCC	L2(7)	Peak fibers 12 to 15 sum
Common NCC Gate	L2(8)	Gate fibers 0 to 3 sum
Front NCC Gate	L2(9)	Gate fibers 4 to 6 sum
Middle NCC Gate	L2(10)	Gate fibers 8 to 11 sum
Rear NCC Gate	L2(11)	Gate fibers 12 to 15 sum
Special NCC	L2(12)	OR of bits(0/1/14/15) of NCC Common fiber 3
Exclusive Common NCC	L2(13)	L2(0) .AND. NOT(L2(5))
Exclusive Middle NCC	L2(14)	L2(2). AND. NOT(L2(5))
NCC Deep	L2(15)	L2(0).AND. L2(6).AND.L2(7).AND. NOT(L2(5))
OEV Hits	L3(0)	Multiplicity fibers 0 to 2 sum
OEV Energy	L3(1)	Peak fibers 0 to 2 sum

Table 4: Description of veto trigger Output Bits sent from the L1Veto boards via the fiber from port 7: **peak** means that the trigger is asserted for the maximum energy sampling above threshold; **gate** means that the trigger is asserted for all samplings with energy above threshold; **hits** means that the trigger is asserted when the hit multiplicity is above threshold. (*) This decision is generated by a dedicated logic module in the Virtex 5 firmware called MB_COSMIC_LOGIC block by first requiring the coincidence of hits at both ends of the MB readout chambers and then counting all hits in the inner (top plus bottom) and outer (top plus bottom) MB barrel layers. When both inner and outer hit multiplicities are above threshold, the MB Cosmic decision bit is set to 1.

Veto Fiber	Output Bit	Description
CC04 Energy	R0(0)	Peak fibers 0 to 1 sum
CC04 Hits	R0(1)	Multiplicity fibers 0 to 1 sum
CC03 Energy	R0(4)	Peak fibers 4 to 5 sum
CC03 Hits	R0(5)	Multiplicity fibers 4 to 5 sum
CC05 Energy	R0(8)	Peak fibers 8 to 9 sum
CC05 Hits	R0(9)	Multiplicity fibers 8 to 9 sum
CC06 Energy	R0(12)	Peak fibers 12 to 13 sum
CC06 Hits	R0(13)	Multiplicity fibers 12 to 13 sum
new BHCV Total	R1(7)	Peak fibers 0 to 15 sum
new BHCV Hits	R1(8)	Gate fibers 0 to 15 sum
Partial IB Energy Sum	L4/L5(15:0)	Energy sum fibers 8 to 15
Total IB Energy Sum*	L5(15:0)*	Energy sum fibers 0 to 15*

Table 5: Description of veto trigger Output Bits sent from the L1Veto boards via the fiber from port 7: **peak** means that the trigger is asserted for the maximum energy sampling above threshold; **hits** means that the trigger is asserted when the hit multiplicity is above threshold. (*) The last entry is used with an alternative IB veto boards configuration in which only L1Veto board in slot 16 of the L1 Veto crate is installed. In this configuration, enabled by bit(1) of VME register 0x2C, the L1Veto board has IB input fibers 0-6 and 8-15 connected. The IB fiber from ADC A17-9 is connected directly to input L4 of the left Master board. The "Total IB Energy Sum" is calculated inside the NEW_MASTER_VETO block by and aligning adding together the energy from the L4 and L5 input fibers.

4 Control Registers

This section list the VME registers defined in the L1 TRIGGER board firmware to enable different boards functionality, set the thresholds used in the veto trigger bit definition and report on the status of internal diagnostic counters. Table 6 gives an overview of the different registers while tables 7 and 8 go in the details of the enables and status register.

(a) The "TLK Errors Count" VME register reports the number of TLK errors. A TLK error is defined as an 8ns sampling in which both the RX_DV and RX_ER outputs of the TLK chip are high. The "Single-Bit Error Count" reports the number of 8-ns samplings for which the fiber data received the ADC generated random sequence is different from the internally random generated sequence [6]. Both counts are only for fiber enabled via the 'Set Error Counter Mask' register (0xBC).

(b) The "TLK Error Position" VME register reports which input fiber had the last TLK error by driving high the bit corresponding to the input fiber number (that is bit(i)=1 if input fiber *ith* had the last TLK error). Similarly, the "Single-Bit Error Position" register reports which input fiber had the last random sequence error. In this case the bit corresponding to the fiber number is shifted up by 16. Position errors are reported only for fibers previously enabled via the 'Set Error Counter Mask' register (0xBC).

(c) Bit(0) of this register selects whether to use the backplane or front-panel versions of the LIVE and L1A signals inside the firmware. Its default value is 0, meaning that the backplane signals are used. The status of this signal is monitored via bit(3) of the status register 0xEC.

(d) Total number of L1A seen from the last board reset.

(e) Read number of system clock cycles from LIVE before a non zero value is seen. Bits(7:0) read the count for the local energy sum before it is injected into the daisy-chain driver. Bits(23:16) read the count for the data received from the backplane at the daisy-chain input. In order for these counts to be correct, the board must be in calibration mode by setting the "Daisy-Chain Calibration Enable" bit(24) of register 0xCC high.

(f) Simulate the content of the daisy-chain input(output) when bit 16(17) of register 0xCC is set to 0. Default value is zero.

(g) Set the delay for the local energy sum data so that it aligns with the daisy-chain inputs. Must be set equal to the difference between the two delays returned by register 0x5C when the board is in calibration mode (see note (e)).

(h) Set the maximum number of TLK errors allowed in one spill. At power up or after a firmware reset, the default value for this register is 0x20. When the number of TLK errors goes over this maximum, bit(7) of Status Register 0xEC goes high until the end of LIVE.

[6] The random generated sequence is enabled by LIVE in the L1 TRIGGER firmware. On the ADC side, it also starts with LIVE if the `loop_back_enable_2p5` register is set to 1.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read TLK Error Count$^{(a)}$	16	RO	0xC	data[15:0]
Read Single-bit Error Count$^{(b)}$	16	RO	0xC	data[31:16]
Read TLK Error Position$^{(a)}$	16	RO	0x1C	data[15:0]
Read Single-Bit Error Position$^{(b)}$	16	RO	0x1C	data[31:16]
Select LIVE/L1A source$^{(c)}$	1	RD	0x2C	data[0]
Select Veto Enables (see Table 7)	3	RD	0x2C	data[3:1]
Read L1A Counter$^{(d)}$	16	RO	0x3C	data[15:0]
Counters Reset$^{(z)}$	1	WO	0x4C	data[0]
Daisy-chain Calibration Result$^{(e)}$	16	RO	0x5C	data[23:16,7:0]
Set Input Daisy-chain Energy$^{(f)}$	24	RW	0x6C	data[23:0]
Set Output Daisy-chain Energy$^{(f)}$	24	RW	0x7C	data[23:0]
Set adder-tree delay$^{(g)}$	7	RW	0x8C	data[6:0]
Set max. TLK errror count$^{(h)}$	16	RW	0x9C	data[15:0]
Set Delay for LIVE$^{(i)}$	7	RW	0xAC	data[6:0]
Set Error Counter Mask$^{(j)}$	32	RW	0xBC	data[31:0]
Set Fiber Enables$^{(k)}$	16	RW	0xCC	data[15:0]
Set Veto Enables (see Table 7)	16	RW	0xCC	data[31:16]
FIFO Reset$^{(z)}$	1	WO	0xDC	data[0]
Read Status bits (see Table 8)	32	RO	0xEC	data[31:0]
Firmware VME Reset$^{(z)}$	1	WO	0xFC	data[0]
Read Daisy-Chain Single-bit Error$^{(p)}$	32	RO	0x4	data[31:0]
Set Single Crate Thresholds$^{(q)}$	18	RW	0x14	data[17:0]
Set Thresh. for Veto Sum of fibers 0-15$^{(r)}$	20	RW	0x24	data[19:0]
Set Thresh. for Veto Sum of fibers 0-6$^{(r)}$	20	RW	0x34	data[19:0]
Set Thresh. for Veto Sum of fibers 8-15$^{(r)}$	20	RW	0x44	data[19:0]
Read Input Delay Calibration$^{(s)}$	8	RO	0x54	data[7:0]
Set Pedestal Subtraction Energy$^{(t)}$	20	WR	0x64	data[19:0]
Set Thresh. for Veto Sum of fibers 0-3$^{(r)}$	20	RW	0x74	data[19:0]
Set Thresh. for Veto Sum of fibers 4-6$^{(r)}$	20	RW	0x84	data[19:0]
Set Thresh. for Veto Sum of fibers 8-11$^{(r)}$	20	RW	0x94	data[19:0]
Set Thresh. for Veto Sum of fibers 12-15$^{(r)}$	20	RW	0xA4	data[19:0]
Set Thresh. for Veto Multiplicity$^{(u)}$	24	RW	0xB4	data[23:0]
Set Output Fiber Bit Enable$^{(v)}$	16	RW	0xC4	data[31:16]
Set Thresh. for Cosmic Veto Multiplicity $^{(u)}$	3x5	RW	0xD4	data[23:0]
Set Time of veto bits Counter to FIFO$^{(**)}$	16	RW	0xE4	data[15:0]
Set Thresh. for Veto Multiplicity by 4$^{(u)}$	32	RW	0xF4	data[31:0]
Set Thresh. for new BHCV Multiplicity$^{(u)}$	2	RW	0x140	data[1:0]
Set Thresh. for BPHV Multiplicity$^{(u)}$	4	RW	0x150	data[3:0]
Set Thresh. for IB energy$^{(r)}$	16	RW	0x170	data[15:0]

Table 6: List of User Defined Registers defined for the L1 TRIGGER board.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Set Input Fiber Mask$^{(k)}$	16	RW	0xCC	data[15:0]
Set Daisy-Chain Input Enable$^{(k)}$	1	RW	0xCC	data[16]
Set Daisy-Chain Output Enable$^{(k)}$	1	RW	0xCC	data[17]
Set Single Crate Threshold$^{(l)}$	1	RW	0xCC	data[18]
Set Master Veto board $^{(m)}$	1	RW	0xCC	data[20]
Set Left vs Right Master Veto$^{(m)}$	1	RW	0xCC	data[21]
Set 500 MHz Hit Adder$^{(n)}$	1	RW	0xCC	data[22]
Set L1Veto board flavor$^{(n)}$	1	RW	0xCC	data[23]
Daisy-Chain Calibration Enable$^{(o)}$	1	RW	0xCC	data[24]
Enable veto counter to FIFO$^{(**)}$	1	RW	0xCC	data[25]
Set CV L1Veto board$^{(n)}$	1	RW	0xCC	data[26]
Set OEV L1Veto board$^{(n)}$	1	RW	0xCC	data[27]
Set NCC L1Veto board$^{(n)}$	1	RW	0xCC	data[28]
Set MB_FB L1Veto board$^{(n)}$	1	RW	0xCC	data[29]
Set BH L1Veto board$^{(n)}$	1	RW	0xCC	data[30]
Set COLLAR L1Veto board$^{(n)}$	1	RW	0xCC	data[31]
Set IB L1Veto board$^{(n)}$	1	RW	0x2C	data[1]
Set 15 fibers for IB L1Veto board$^{(n)}$	1	RW	0x2C	data[2]
Set old BPCV L1Veto board$^{(n)}$	1	RW	0x2C	data[3]

Table 7: List of board enables and masks defined via registers 0xCC and 0x2C. At power up or after a board reset, the default value is 0x3FFFF and 0x0, respectively. (**) Bit(25) of register 0xCC enables the recording of veto bit counters to a 32K deep 32-bit FIFO. The counter is recorded in the FIFO every N sampling, where N is programmable and equal to the number of 8ns cycle set by register 0xE4. The FIFO can be read via register 0x100_0000.

Status of LIVE$^{(c)}$	1	RO	0xEC	data[0]
Status of Bkpln LIVE$^{(c)}$	1	RO	0xEC	data[1]
Status of Front panel Live$^{(c)}$	1	RO	0xEC	data[2]
Status of LIVE/L1A Source Select$^{(c)}$	1	RO	0xEC	data[3]
Status of Input FIFOs Full Line$^{(w)}$	1	RO	0xEC	data[4]
Status of K0TO_ERROR Signal$^{(x)}$	1	RO	0xEC	data[5]
Status of Internal Energy Sum Ovfl.$^{(t)}$	1	RO	0xEC	data[6]
Status of TLK Error Counter$^{(h)}$	1	RO	0xEC	data[7]
Board Revision$^{(y)}$	4	RO	0xEC	data[19:16]
Firmware Revision$^{(y)}$	4	RO	0xEC	data[23:20]
Firmware Version$^{(y)}$	4	RO	0xEC	data[27:24]
Board Type$^{(y)}$	4	RO	0xEC	data[31:28]

Table 8: Content of Status Register bits for the L1 TRIGGER Board.

(i) Set the delay between LIVE and ENABLE_SUM. ENABLE_SUM is the signal that enables data from the L1 fiber to get out of the SUM_ALIGNMENT block. At power up or after a board reset, the default value for this register is 0x3C (dec 60). This delay has to be set larger than the value measured by the "Input Delay Calibration" register 0x54 (see note (s)). At the same time, it cannot be larger than 0x80 (dec 128) to prevent the FIFO inside the the SUM_ALIGNMENT block from overflowing. It will reset itself automatically to the default value if a value greater than 0x80 is downloaded.

(j) Bit(15:0) are used as a mask to enable data from the *ith* input fibers into the TLK/Single-bit Error counter logic (see notes (a) and (b)). Bit(31:16) are used as a mask to select which of the input fibers are connected to the daisy-chain during daisy-chain integrity tests (see note (p)). At power up or after a board reset, the default value for these bits is all 0.

(k) Bit(i) (i=0 thru 15) are used as a mask to enable data from the *i-th* input fiber into the firmware. Bit(16/17) is used to enable the input/output daisy-chain data into/out of the firmware. The default value for all these bits is 1.

(l) When bit(18) of register 0xCC is low (default), the total calorimeter energy is passed to the P3 daisy-chain for the L1 Trigger decision. When this bit is high, the local energy sum is compared to a local threshold, set by register 0x14, and the resulting ADC crate trigger decision (CSUM or Regional Trigger) is passed to the P3 daisy-chain. From firmware v4.4 up, this enable is obsolete. A separate path is used to pass the Regional Trigger to Master MACTRIS so that both the total energy and the CSUM trigger decision from all of the CsI L1TRG boards can be used in the final L1A decision. A CSUM trigger is generated at the peak of the local energy sum above threshold and passed as a 3-clk long pulse to the K0TO_PTP1 backplane signal [7].

[7]K0TO_PTP1 is a point-to-point P3 backplane signal connecting each of the slots in the daisy-chain to a separate pin in slot 12 of the P3 backplane. It allow signals from individual L1TRG boards to be sent to/from

(m) When bit(20) of register 0xCC is high, the Master Veto flavor of the L1 TRIGGER board firmware is selected and all daisy-chain bits (23:0) are driven to the P3 backplane (bit(23:18) for veto bit and bit(17:0) for the energy sum). When bit(20) of register 0xCC is low (default) and bit(23) of register 0xCC is low (see next note (n)), the L1TRG flavor of the L1 TRIGGER board is selected and bit(17:0) are driven with the local energy sum plus the energy received from the previous board in the daisy-chain while bit(23:18) are passed to the output daisy chain unchanged. Bit(21) of register 0xCC set to 1/0 enables the Left vs Right Master Veto board, which are the boards installed slot 4 vs 20 of the L1 Trigger crate. The firmware inside the NEW_MASTER_VETO block can process data from different veto detector input ports and generate the P3 backplane bits as specified in Table 3.

(n) When bit(23) of register 0xCC is high, the L1Veto flavor of the L1 TRIGGER board firmware is selected (bit(23), whose default value is 0, is used together with bit(20) of register 0xCC to indicate L1TRG board firmware, as per note (m)). Bit(31:24) of register 0xCC and bit(3:1) of register 0x2C [8] are used to specify the L1Veto board output, that is how the input fiber data is used by the NEW_L1VETO_LOGIC block to generate the bit sent out via the port 7 output fiber. See Tables 2, 4 and 5 for the details of the L1Veto board I/Os assignments and mapping. Bit(31:16) of register 0xC4 is the mask for the output fiber bits. The default value for all of these bits is 0.

(o) Bit(24) of register 0xCC high sets the board in calibration mode. In this mode, the time for LIVE to propagate thru the system is measured by calculating how long it takes to observe the input fiber alignment word, 0xFEFE, at different points inside the firmware. After these delays are calibrated, set bit(24) must be set low. This masks out the alignment word before it enters the Energy Adder or the L1 Veto block, and avoids spurious triggers.

(p) This register is used when doing stand-alone L1 TRIGGER board tests or when testing the integrity of the daisy-chain in P3 backplane. It reports the number of 8-ns samplings for which the data generated by the local energy sum logic does not agree with the sum of ADC generated random sequence data connected to the adder tree inputs. Bit(15:0) report errors for the output of the single board adder tree while bit(31:16) report for the comparison of the input daisy-chain. Bit(31:16) of register 0xBC are used as a mask to select which of the input fibers are connected to the daisy-chain.

(q) This register sets the local energy threshold used for the CSUM, or regional, trigger decision.

(r) These registers set the thresholds for the partial energy sums peak and gate decision used by the L1Veto board logic to generate the output fiber trigger bits. All thresholds are 20-bit value, with a default of 0xF_FFFF, with the exception of register 0x170 used in the

MACTRIS+.

[8] Special cases: **bit (2) of register 0x2C** enables an alternative configuration for the IB veto readout for which a single IB L1 veto board in slot 16 of the L1 Veto crate is used. In this case, fibers from ADC17-3 to A17-9 have to be connected to input 0-6 of the IB veto board and fiber from ADC17-10 to A17-18 to inputs 7-15. The leftover fiber from ADC17-9 has to be connected directly to input 4 of the left Master Veto board in slot 4 of the L1 Trigger crate; **bit(22) of register 0xCC** is used to identifiy L1Veto board receiving 500 MHz ADC data. For these boards, the hit multiplicity is calculate using the algorithm in Section 2.

IB energy sum trigger. This register is only 16-bit as it is used to compare the energy coming in via the output fibers of the IB L1veto boards. Its default value is 0xFFFF.

(s) This register reports the delay between LIVE and the capture of the 0xFEFE alignment word by all of the input fibers specified by the "Set Fiber to Adder Enables" register (0xCC). This is a measure of the maximum delay between LIVE being generated by MACTRIS+ and ADC energies being received by the L1 TRIGGER board. It determines the minimum value allowed for the "Set Delay for LIVE" register (0xAC) during physics data. Note that in order for this delay to be properly measured, the board must be in calibration mode (i.e. bit(24) of register 0xCC high) and the delay of ENABLE_SUM itself has to be set to its maximum value (0x80) via register 0xAC (see note (i).

(t) This register sets the value of the pedestal energy to be subtracted from the raw energy raw calculated by the ENERGY_ADDER block in order to prevent overflowing the 18 bits allocated in the P3 daisy-chain when no pedestal subtraction is done in the ADCs. The default value is 0. The value of the raw energy sum can be readout via the energy monitoring register 0xB8. The pedestal subtraction is enabled when the board is not in calibration mode i.e. when bit(24) of register 0xCC is low. The energy sum overflow condition, calculated as the OR of the pedestal subtracted energy bits 16 thru 19, is monitored via bit(6) of the status register 0xEC.

(u) These registers set the thresholds for the counter of veto hit multiplicity used in the L1Veto logic. Bit(7:0) of register 0xB4 set the thresholds for sum over input fibers 0 to 15, bit(15:8) for the sum over input fibers 0 to 6 and bit(23:16) for the sum over input fibers 8 to 15. Bit(7:0) of register 0xF4 set the thresholds for sum over input fibers 0 to 3, bit(15:8) for the sum over input fibers 4 to 6, bit(23:16) for the sum over input fibers 8 to 11 and bit(31:24) for the sum over input fibers 12 to 15. Finally, bit(4:0) of register 0xD4 set the thresholds for the hit multiplicity for the Inner MB, bit(12:8) for the Outer MB and bit(27:24) for the MB Cosmic decision (see description in Table 4). The default for all of these bits is 1.

(v) Bit(31:16) of register 0xC4 is the mask for the output bits of the L1Veto board port 7 fiber. All enabled bits are ORed together inside the Master Veto board to produce the final veto detector trigger bit. N.B. Bit(15:0) were used in firmware v4.6 and below to add an extra 16 nsec delay for input fiber data from small vs large crystals and are presently unused.

(w) This signal report the logical OR of the FULL outputs for all of the FIFOs inside the SUM_ALIGNMENT block.

(x) This signal is high when any TLK error from an enabled input fiber is detected.

(y) Bit(31:16) of register 0xEC contain information about the board type and firmware version, namely: bit(19:16) encode the L1 TRIGGER board hardware version type (0x0 for old Trigger board, 0xB for revB board, 0xC for revC TRIGGER board); bit(23:20) and bit(27:24) encode the firmare version and revision number; bit(31:28) encode a unique value for each 9U VME trigger board in the system (0x1 for L1 Trigger, 0x2 for L2 Trigger, 0x4 for MACTRIS, 0x5 for MACTRIS+, 0x3 for Fanout)

(z) By writing 1 to bit(0) of these registers we reset different parts of the firmware. More specifically, 0x4C resets all of the counters to zero, 0xDC clears the contents of the FIFOs and 0xFC resets all of the VME controlled registers to their default value.

5 Energy Diagnostic Registers

The L1 TRIGGER firmware has multiple registers designed to capture the energy of the incoming fibers as well as the progression of the energy sum inside the firmware. They are listed in Tables 9 and 10, respectively.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read fiber 0	32	RO	0x0	data[31:0]
Read fiber 1	32	RO	0x10	data[31:0]
Read fiber 2	32	RO	0x20	data[31:0]
Read fiber 3	32	RO	0x30	data[31:0]
Read fiber 4	32	RO	0x40	data[31:0]
Read fiber 5	32	RO	0x50	data[31:0]
Read fiber 6	32	RO	0x60	data[31:0]
Read fiber 7	32	RO	0x70	data[31:0]
Read fiber 8	32	RO	0x80	data[31:0]
Read fiber 9	32	RO	0x90	data[31:0]
Read fiber 10	32	RO	0xA0	data[31:0]
Read fiber 11	32	RO	0xB0	data[31:0]
Read fiber 12	32	RO	0xC0	data[31:0]
Read fiber 13	32	RO	0xD0	data[31:0]
Read fiber 14	32	RO	0xE0	data[31:0]
Read fiber 15	32	RO	0xF0	data[31:0]

Table 9: List of the single fiber energy monitoring registers.

The 32 bit of data read out for each fiber in Table 9 contain the following info:

- bits (31:16) are the energy data readout at the input of each fiber, ie the energies generate by the TLK receiver outputs registered at the recovered clock. When LIVE is low, they should read the IDLE word 0x50BC.
- bits (15:0) are the energy data for each fiber after being aligned with system clock. These are also the inputs to the ENERGY_ADDER, NEW_L1VETO_LOGIC and NEW_MASTER_VETO blocks. When LIVE is low, they will read zero. When LIVE is high, they will have non zero reading only when they are enabled by "Input Fiber Mask" via bit(15:0) of VME register 0xCC.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read sum of fibers 0 thru 3	18	RO	0x8	data[17:0]
Read sum of fibers 4 thru 7	18	RO	0x18	data[17:0]
Read sum of fibers 9 thru 12	18	RO	0x28	data[17:0]
Read sum of fibers 13 thru 15	18	RO	0x38	data[17:0]
Read sum of fibers 0 thru 7	19	RO	0x48	data[18:0]
Read sum of fibers 8 thru 15	19	RO	0x58	data[18:0]
Read sum of MB inner hits	5	RO	0x78	data[4:0]
Read sum of MB outer hits	5	RO	0x88	data[4:0]
Read raw sum fibers 0 thru 15	20	RO	0xB8	data[19:0]
Read daisy-chain input 24 bits	24	RO	0xC8	data[23:0]
Read sum energy and L1 veto bits	24	RO	0xD8	data[23:0]
Read sum of internal & daisy-chain bits	24	RO	0xE8	data[23:0]
Read daisy-chain output 24 bits	24	RO	0xF8	data[23:0]

Table 10: List of the registers monitoring the total energy at various points inside the firmware and MB hit multiplicity. Sum fibers are at the exit of the ENERGY_ADDER block, before pedestal subtraction.

6 L1 TRIGGER Schematics Description

Sheet 1 Input and Output Clock logic; Heart-bit and VME Activity LED Logic. Reset logic.

Sheet 2 VME Interface; Firmware Version bits; User defined commands 0xnC (n=0 thru F); 0xCC enables and 0xEC status register definiton.

Sheet 3 LIVE and L1A Control Logic; ENABLE_SUM Logic and L1A Counter; 0x2C enables

Sheet 4 TLK Mask and TLK Error Counter Logic. Single input fiber monitoring registers 0xn0 and energy monitoring registers 0xn8

Sheet 5 SUM_ALIGNMENT blocks for fiber data alignment.

Sheet 6 Fiber Enable to Adder Tree and Veto Logic

Sheet 7 Input energy diagnostic registers for fibers 0 thru 7

Sheet 8 Input energy diagnostic registers for fibers 8 thru 15

Sheet 9 Adder Tree and Local Energy Sum Logic; Energy pedestal subtraction logic; CRATE SUM decision logic.

Sheet 10 Daisy-Chain Delay Calibration Logic and Input Fiber Alignment Calibration Logic

Sheet 11 Partial Energy Sum and Veto Bit Counters Diagnostic Logic.

Sheet 12 Random Sequence Generator; Random Sequence Single-bit Error Counters.

Sheet 13 Random Sequence Single-bit Error Detection Logic.

Sheet 14 Adder Tree Single-bit Error Detection Logic

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Sheet 16 VME Command Registers 0xn4; CRATE SUM peak trigger logic, shaping and delay.

Sheet 17 TLK control signals definition; L1Veto fiber Alignment Logic; Veto Bit Counters; Veto Timing FIFO Enable.

Sheet 18 NEW_MASTER_VETO block and veto bits daisy-chain drivers.

Sheet 19 Single fiber hits adders.

Sheet 20 NEW_L1VETO_LOGIC and MB_COSMIC_LOGIC blocks.

Sheet 21 VME Registers for veto energy and multiplicity bit thresholds; Veto timing FIFO

Sheet 22 VME Registers for BHCV and IB veto thresholds 0x1n0.

Sheet 23 Firmware Versioning History