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# L2 (COE) Mactris Board VME Address Space

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This document specifies the VME address space defined for the L2 COE Mactris board, also known as COE Mactris. This document works with the firmware binary version v3.1 and above and document "L2 Trigger Board VME Address Space v3.3".

There are four types of registers depending on functionalities and access: (1) *command registers* (with address 0xXC, where X=0,1...,F) that include board level mode monitors and configuration settings. Most of command registers are both writeable and readable.

(2) *configuration registers* (with address 0xX4), which define parameters used in the COE decision. They are all both writeable and readable.

(3) *status registers* (with address 0xX8), which read the status of FIFOs and counters, and are readonly.

(4) *Bulk readout registers* (with address 0x1X00000 (5 zeros)), which can be readout via DMA (direct memory access) using a different vme utility vme7700_block_dma.

# 1 Command Registers

| Name | Size (bit) | VME Access | VME Addr | Bit Assignment |
|---|---|---|---|---|
| Undefined | 32 | WR | 0xC | data[31:0] |
| VME live$^{(*)}$ | 1 | WO | 0x1C | data[0] |
| Undefined | 32 | WR | 0x2C | data[31:0] |
| Send VME trigger(*) | 1 | WO | 0x3C | data[0] |
| Reset Counter | 1 | WO | 0x4C | data[0] |
| Left daisy chain data write | 1 | WR | 0x5C | data[0] |
| Right daisy chain data write | 1 | WR | 0x6C | data[0] |
| Undefined | 32 | WR | 0x7C | data[31:0] |
| Undefined | 32 | WR | 0x8C | data[31:0] |
| Undefined | 32 | WR | 0x9C | data[31:0] |
| Undefined | 32 | WR | 0xAC | data[31:0] |
| Undefined | 32 | WR | 0xBC | data[31:0] |
| Mode configuration (see Table2) | 32 | WR | 0xCC | data[31:0] |
| Undefined | 32 | WR | 0xDC | data[31:[0] |
| Global status (see Table3) | 16 | RO | 0xEC | data[15:0] |
| FIFO version | 16 | RO | 0xEC | data[31:16] |
| Firmware Reset (non-FIFO) | 1 | WO | 0xFC | data[0] |

Table 1: L2 Mactris Board Command Registers Bitmap (registers with an $(*)$ are defined to mimic Master MACTRIS features and included solely for the purpose of testing the L2 board in the Michigan test stand.)

| Bit | Definition |
|---|---|
| 16 | Enable Left Daisy Chain Data |
| 17 | Enable Right Daisy Chain Data |
| 26$^{(*)}$ | Enable Random Trigger Generator |
| 28$^{(*)}$ | Disable coe |
| 29$^{(*)}$ | Enable Even Spaced L1A Simulated triggers |
| 31$^{(*)}$ | Enable L2 Readout (enable L2 input buffer simulator) |

Table 2: Mode Register 0xCC bitfield. Default upon configuration or reset is 0x30000 (registers with an $(*)$ are defined to mimic Master MACTRIS features and included solely for the purpose of testing the L2 board in the Michigan test stand.)

| Bit | Definition |
|---|---|
| 0 | Status of Live (1=on; 0=off) |
| 1 | L2d FIFO fulll |
| 2 | Disable l1a |
| 3 | L2d FIFO empty |

Table 3: Status Register 0xEC bitfield (registers with an (∗) are defined to mimic Master MACTRIS features and included solely for the purpose of testing the L2 board in the Michigan test stand.)

# 2 COE Configutation Registers 0xX4 registers

These are read-write registers used to set parameters for the COE logic and simulated L1A Trigger generation.

| Name | VME Addr | Bit Assignment |
|---|---|---|
| COE (Ex+Ey) LSB | 0x04 | bit[31:0] |
| COE (Ex+Ey) MSB | 0x14 | bit[31:0] |
| COE algorithm$^{(a)}$ | 0x54 | bit[3:0] |
| COE threshold$^{(b)}$ | 0x74 | bit[31:0] |
| Time between evenly space simulated L1A (in 8ns)$^{(*)(c)}$ | 0xA4 | bit[31:16] |
| Number of evenly spaced simulated L1A$^{(*)(c)}$ | 0xA4 | bit[15:0] |
| Random L1a generator threshold$^{(*)(d)}$ | 0xC4 | bit[31:0] |
| Daisy Chain Mask (Bitfield see Table5) | 0xD4 | bit[16:0] |

Table 4: COE Configuration VME Addresses (registers with an (∗) are defined to mimic Master MACTRIS features and included solely for the purpose of testing the L2 board in the Michigan test stand.)

(a) set to 0/1 if L2d decision is made for COE smaller/larger than threshold. Default is 0.
(b) Default is 0x10.
(c) Default is 0x1_0001.
(d) Default is 0xFFFF_FFFF: 0xFFFF_0000 corresponds to about 1 KHz; 0xFFF8_0000 to 4 KHz; and 0xFFF6_4000 to the maximum rate of 9 KHz.

| bit | 13 | 12 | 11 | 10 | 9 | 8 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Slot | 20 | 19 | 18 | 15 | 14 | 13 | 4 | 5 | 6 | 9 | 10 | 11 |

Table 5: Bit definition for Daisy Chain Mask Register 0xD4. Default is 0x3F3F.

# 3 Status Registers 0xX8

These read-only registers used to monitor the system, including counters.

| Name | VME Addr | Bit Assignment |
|---|---|---|
| Left Daisy Chain Data | 0x08 | bit[31:0] |
| Right Daisy Chain Data | 0x18 | bit[31:0] |
| L2 Decision internal counter | 0x28 | bit[31:0] |
| L2 Decision sent to L2 Trigger counter | 0x38 | bit[31:0] |
| L2 Accept internal counter | 0x48 | bit[31:0] |
| L2 Reject internal counter | 0x58 | bit[31:0] |
| COE request to L2 Trigger counter | 0x68 | bit[31:0] |
| L2 Accept sent to L2 Trigger counter | 0x78 | bit[31:0] |
| L2 Reject sent to L2 Trigger counter | 0x88 | bit[31:0] |
| L1 Accept counter | 0x98 | bit[31:0] |

Table 6: Status registers.

# 4 Bulk data Registers 0x1X00000 Registers

Each register is connected to a *K deep FIFO and can be readout via DMA (direct memory access). To read out the FIFO via VME use the command:

./ vme7700_block_dma *read* "slot number" *1X00000* depth

| Name | VME Access | VME Addr | Depth |
|---|---|---|---|
| Et | RO | 0x1000000 | 8k |
| Ex_LSB | RO | 0x1100000 | 8k |
| Ex_MSB | RO | 0x1200000 | 8k |
| Ey_LSB | RO | 0x1300000 | 8k |
| Ey_MSB | RO | 0x1400000 | 8k |
| Ey_MSB_left | RO | 0x1500000 | 8k |
| Ey_MSB_right | RO | 0x1600000 | 8k |
| L2 Decision | RO | 0x1700000 | 8k |

Table 7: Bulk Registers Bitfields.