K0TO Note XXX
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L2 (COE) Mactris Board v5.0 VME Address Space

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This document specifies the VME address space defined for the L2 COE Mactris board v5.0, also known as COE Mactris. The main difference with firmware v4.0 is the implementation of event-by-event COE above and below threshold cuts . This feature requires MACTRIS version v6.0 or above.

There are four types of registers depending on functionalities and access:

(1) *command registers* (addresses 0xXC, where X=0,1...,F) include board level mode monitors and configuration settings. Most of command registers are both writeable and readable.

(2) *configuration registers* (addresses 0xX4, X=0,1...,F) define parameters used in the COE decision and L1A simulation. They are all both writeable and readable.

(3) *status registers* (addresses 0xX8, X=0,1...,F) read various counters.

(4) *bulk readout registers* (addresses 0x1X0_0000, X=0,1...,F), can readout content of FIFOs via DMA (direct memory access).

1 Introduction

Starting from version 5.0 of the firmware, new logic was added to receive the early L1A sent by MACTRIS via the LVDS external input 1. In MACTRIS+ version 6.0, this signal can have three different length to encode the following information: if 3 clocks long, it is a physics event for which a COE above threshold cut has to be applied; if 5 clocks long, it is a physics event for which a COE below threshold cut has to be applied; if 7 clocks long, it is a normalization event for which a COE above threshold cut has to be applied[1]. The length of this signal is decoded in the `coe_thresh_decoder` module and passed to the COE FIFO decision as 0/1 to indicate a COE below/above threshold cut. The decision is then made available to the `L2_decision` block after the final COE sum for the event has been calculated in the `COE_Input_calculator` block.

Another new feature in version v5.0 of the firmware is the `live_detector` block, where we infer the end of LIVE by requiring a large time in between L1A received by MACTRIS. This time is programmable via VME register 0x8C and set by default to a value of 8 nc clocks equal to 0x800_0000, corresponding to about 1 s. Finally, many of the 8K deep FIFO instantiated in the firmware are devoted to save event statistics per spill, as explained in Table 7.

2 Command Registers

Name	Size (bits)	VME Access	VME Addr	Bit Assignment
Read L1A from MACTRIS per spill	32	RO	0xC	data[31:0]
Set VME live$^{(*)}$	1	WO	0x1C	data[0]
Read spill number	32	RO	0x2C	data[31:0]
Send VME trigger(*)	1	WO	0x3C	data[0]
Reset Counters	1	WO	0x4C	data[0]
Left-daisy chain data write	1	WR	0x5C	data[0]
Right-daisy chain data write	1	WR	0x6C	data[0]
Maximum time between L1A	32	WR	0x8C	data[31:0]
Mode configuration (see Table2)	32	WR	0xCC	data[31:0]
Global status (see Table3)	16	RO	0xEC	data[15:0]
Firmware Reset (all bit FIFOs)	1	WO	0xDC	data[0]
FIFO version	16	RO	0xEC	data[31:16]
Firmware Reset (all bit FIFOs)	1	WO	0xFC	data[0]

Table 1: L2 Mactris Board Command Registers Bitmap. Registers with an $(*)$ are defined to mimic Master MACTRIS features and included solely for the purpose of testing the L2 board in the Michigan test stand.

[1]By normalization event we mean an event for which an automatic L2 accept has to be issued. Depending on the firmware in MACTRIS and L2TRG, these events might be dealt by overflowing the COE energy, and thus generating conditions for which an automatic L2 accept is issued.

Bit	Definition
16	Enable left-daisy chain data
17	Enable right-daisy chain data
18	Enable COE algorithm setting via VME
$19^{(*)}$	Enable Automatic L2A
20	Enable counter clear at LIVE end
$26^{(*)}$	Enable random trigger generator
$29^{(*)}$	Enable fixed rate L1A Simulated triggers
31	Enable L1A from MACTRIS

Table 2: Mode Register 0xCC bitfield: default upon configuration or reset is 0x70000. Registers with an $(*)$ are defined to mimic Master MACTRIS features and included solely for the purpose of testing the L2 board in the Michigan test stand.

Bit	Definition
0	Status of Live (1=on; 0=off)
1	L1A Disabled$^{(*)}$
2	L2D FIFO empty
3	L2D FIFO fulll
4	SumE^2 or Thresh^2 overflow
5	L2 Auto Accept
6	COE Algo FIFO empty
7	COE Algo FIFO full

Table 3: Bit definiton for status register 0xEC. Registers with an $(*)$ are defined to mimic Master MACTRIS features and included solely for the purpose of testing the L2 board in the Michigan test stand.

3 COE Configuration Registers

These are read-write registers used to set parameters for the COE logic or simulated L1A Trigger generation.

Name	VME Addr	Bit Assignment
Set COE (Ex+Ey) LSB	0x04	bit[31:0]
Set COE (Ex+Ey) MSB	0x14	bit[31:0]
Set COE algorithm$^{(a)}$	0x54	bit[3:0]
Set above COE threshold$^{(b)}$	0x74	bit[31:0]
Set below COE threshold$^{(b)}$	0x94	bit[31:0]
Set time between simulated L1A (in 8ns)$^{(*)(c)}$	0xA4	bit[31:16]
Set number of simulated L1A$^{(*)(c)}$	0xA4	bit[15:0]
Set random L1A generator threshold$^{(*)(d)}$	0xC4	bit[31:0]
Daisy Chain Mask (Bitfield see Table 5)	0xD4	bit[16:0]

Table 4: COE Configuration VME Addresses. Registers with an $(*)$ are defined to mimic Master MACTRIS features and included solely for the purpose of testing the L2 board in the Michigan test stand.

(a) if set to 0/1, L2d decision is made for COE smaller/larger than threshold. If set to 2, the L2d decision is force to be L2A/L2R on alternative events. Default is 0.
(b) Default is 0x0.
(c) Default is 0x1_0001.
(d) Default is 0xFFFF_FFFF: 0xFFFF_0000 corresponds to about 1 KHz; 0xFFF8_0000 to 4 KHz; and 0xFFF6_4000 to the maximum rate of 9 KHz.

bit	13	12	11	10	9	8	5	4	3	2	1	0
Slot	20	19	18	15	14	13	4	5	6	9	10	11

Table 5: Bit definition for Daisy Chain Mask Register 0xD4: if 1/0, that slot is included/excluded in the COE calculation. Default is 0x3F3F.

4 Status Registers

These read-only registers are used to monitor the status of the COE calculation or the value of different internal counters.

Name	VME Addr	Bit Assignment
Left Daisy Chain Data	0x08	bit[31:0]
Right Daisy Chain Data	0x18	bit[31:0]
L2 Decision internal counter	0x28	bit[31:0]
L2 Decision sent to L2 Trigger counter	0x38	bit[31:0]
L2 Accepts internal counter	0x48	bit[31:0]
L2 Rejects internal counter	0x58	bit[31:0]
L2 Accepts sent to L2 Trigger counter	0x68	bit[31:0]
L2 Rejects sent to L2 Trigger counter	0x78	bit[31:0]
Daisy chain sumE requests to counter	0x88	bit[31:0]
Daisy chain LSB sumEx requests to counter	0x98	bit[31:0]
Daisy chain MSB sumEx requests to counter	0xA8	bit[31:0]
Daisy chain LSB sumEy requests to counter	0xB8	bit[31:0]
Daisy chain MSB sumEy requests to counter	0xC8	bit[31:0]
Above COE threshold decisions counter	0xD8	bit[31:0]
Below COE threshold decisions counter	0xE8	bit[31:0]
Normalization Event decisions counter	0xF8	bit[31:0]

Table 6: Status Registers.

5 Bulk Data Registers

Each register is connected to a 8K deep FIFO than can be readout via DMA (direct memory access). To read out the FIFO, use the VME command:

./vme7700_block_dma *read* "slot number" *1X00_000* depth

Name	VME Access	VME Addr	Depth
Event-by-Event sumE	RO	0x100_0000	8k
Normalization Events per Spill	RO	0x110_0000	8k
Above COE Threshold Events per Spill	RO	0x120_0000	8k
Below COE Threshold Events per Spill	RO	0x130_0000	8k
MACTRIS L1A per Spill	RO	0x140_0000	8k
L2A per Spill	RO	0x150_0000	8k
L2R per Spill	RO	0x160_0000	8k
Event-by-Event L2 Decision	RO	0x170_0000	8k

Table 7: Bulk Registers Bitfields.