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L2 Trigger Board VME Address Space

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This document specifies the VME address space defined for the L2 Trigger boards (Virtex 5: v3.50 and above, Virtex 4: v9.1 and above). This document works with "L2 Mactris Board VME Address Space v3.2".

There are four types of registers depending on their functionalities and data access:

(1) *command registers* (with address 0xXC, X=0,1...,F) which include board mode and configuration settings. Most of the command registers are both writeable and readable.

(2) *data spy registers* which show real-time data present on INPUT_FIFO inputs and outputs (ie DUMP_FIFO input), DUMP_FIFO, LENGTH_FIFO and COE_HEADER_FIFO output. They are readonly.

(3) *status registers* which read the status of counters and other miscellaneous diagnostic registers. They are readonly.

(4) *fifo registers* (with address 0x1X0_0000, X=0,1...,F), which dump selected FIFOs contents. They are readonly.

1 Command Registers

Table 1: List of Command Registers for the L2 Trigger Board

Name	Size (bit)	VME Access	VME Addr	Bit Assignment
Memory dump	1	WO	0xC	data[0]
Number of packets written into Memory	32	RO	0x1C	data[31:0]
Virtex4 reset	1	WO	0x2C	data[0]
Number of packets readout from Memory	32	RO	0x3C	data[31:0]
Interpacket delay for readout	32	WR	0x4C	data[31:0]
Virtex4 version	32	RO	0x5C	data[31:0]
Enable EMAC and send slot number	1	WO	0x6C	data[0]
Packet wrapping enable$^{(\star)}$	1	WR	0x7C	data [16]
Input fiber mask	16	WR	0x7C	data[15:0]
Daisy chain input enable	1	WR	0x8C	data[0]
Daisy chain output enable	1	WR	0x8C	data[1]
L2 bypass (force automatic L2A)	1	WR	0x8C	data[2]
COE bypass (for veto boards)	1	WR	0x8C	data[3]
Simulation configuration (see Table 2)	32	WR	0x9C	data[31:0]
Number of Ethernet packets sent out	32	WR	0xAC	data[31:0]
Undefined	32	WR	0xBC	data[31:0]
ADC Nwidth (for simulation only)	4	WR	0xCC	data[3:0]
FIFO Reset	1	WO	0xDC	data[0]
Virtex5 status (see Table 3)	16	RO	0xEC	data[15:0]
Virtex5 firmware version	16	RO	0xEC	data[31:16]
Firmware Reset (non-FIFO)	1	WO	0xFC	data[0]

($\star$) When bit(16) of address 0x7C is set to 1, up to 4 ADC packets are wrapped into a single Ethernet packet, according to the following scheme: ADC packets from inputs 0,1,2 and 3 are wrapped in the first Ethernet packets, 4,5,6, and 7 in the second, 8,9,10 and 11 in the third, and 12,13,14 and 15 in the fourth. The enable mask is set in bit(15:0) of register 0x7C.

Table 2: Simulation configuration register (0x9C) bitmap. Default value: 0x40040006 (i.e. no compression and packet length equal to 1024 for all fibers). **N.B.: Any setting bit is enabled ONLY when the bit(2)=1.**

Bit	Definition	Value
1	L2a	1: simulated L2a (default); 0: system data
2	data	1: simulated data (default); 0: system data
3	WithCOE	disabled (i.e. always 1: with COE words)
4	IsCompress	1: with, 0; w/o compression (default)
[19,8]	payload length	no. energy words for input channels 0-7
[31,20]	payload length	no. energy words for input channels 8-15

Table 3: Virtex 5 Status Register (0xEC) bitmap. Default value: 0xF200. Any other value, especially in between SPILLs, is an indication of a problem. In particular if bit[12] is 0, that board has stopped taking data.

Bit	Definition
0	v2v_irq $^{(a)}$
1	v2v_full $^{(b)}$ (= $\overline{KOTO\_ERROR}$)
2	emac_fifo_full $^{(c)}$
3	some_input_fifo_full $^{(d)}$
4	L2a_seen $^{(e)}$
5	L2r_seen $^{(e)}$
6	l1a_disable $^{(f)}$ (= $\overline{\text{KOTO\_FULL}}$)
7	L2_req_seen$^{(g)}$ (= $\overline{\text{KOTO\_RSVD1}}$)
8	coe_sent $^{(h)}$ (= $\overline{\text{KOTO\_OC\_RSVD}}$)
9	coe_empty $^{(i)}$ (= $\overline{\text{KOTO\_PTP1}}$)
10	dump_ready $^{(j)}$ (= KOTO_PTP2)
11	auto_accept $^{(k)}$
12	coe_start $^{(l)}$
13	L2 Decision FIFO empty $^{(m)}$
14	V2V DATA FIFO empty $^{(m)}$
15	V2V ADDR FIFO empty $^{(m)}$

(a) This signal is driven by the Virtex 4 when the 2K deep V2V FIFO is almost full (i.e. 18 more addresses to go).

(b) This is an Open Collector (OC) signal sent to Master MACTRIS. It is driven by the Virtex 4 when the number of addresses written to the memory has reached 98.5% of full capacity.

(c) This is driven by the Virtex 4 when the 2K deep Ethernet FIFO is full.

(d) This goes high if any input fifo gets full. Cleared by a fifo reset (ie. write 0xdc 1).

(e) These indicate that L2 MACTRIS has sent a L2A_EN with L2A high (L2A) or low (L2R).

(f) This is an OC signal sent to Master MACTRIS when any Input FIFO is about to get full. It disables any further L1A trigger.

(g) This is a bussed signal sent from L2 MACTRIS to indicate that the COE data should be put in the P3 bus.

(h) This is an OC signal sent to L2 MACTRIS when all COE_header FIFOs are not empty.

(i) This is a point-to-point signals between each daisy-chain L2 Trigger slot and L2 MACTRIS. It indicates that none of the dump FIFOs are empty.

(j) This are a point-to-point signals between each daisy-chain L2 Trigger slot and L2 MACTRIS. It indicates that all dump FIFOs are done receiving one packet.

(k) Set when any masked input fibers report L2 Automatic bit in COE word.

(l) This signal is initialized HIGH. It is needed to start the COE Manager state machine, together with INPUT_FIFO not being empty. Cleared by any DUMP FIFO done (all words in a packet have been written to DUMP FIFO). Reset HIGH either by TRIGGER_DONE (issued by MUX when one full trigger has been processed) or by L2R_TRIGGER_DONE (delayed version of a L2 Reject).

(m) These FIFO empty signals should be all high during normal data taking. If not, they indicate that some data has not been fully read out of the INPUT_FIFOs. They should be correlated with Frontend FIFOs status bits (see Tables 6 and 7).

2 Data Spy Registers

These RO registers are used for data spying, to verify that the fibers are properly connected and that the packets are properly handled by the Frontend Module. In normal conditions, each input INPUT_FIFO input should read 0x50bc (synced fiber idle word) when data transfer is idle. After a successful data transfer to memory, the INPUT_FIFO output (input of DUMP_FIFO) should be the last COE word of the last ADC packet received by the fiber and the DUMP_FIFO output should be 0x1234.

Name	VME Addr	Bit Assignment
INPUT_FIFO input fiber 1/0	0x0	bit[31:16]/[15:0]
INPUT_FIFO input fiber 3/2	0x10	bit[31:16]/[15:0]
INPUT_FIFO input fiber 5/4	0x20	bit[31:16]/[15:0]
INPUT_FIFO input fiber 7/6	0x30	bit[31:16]/[15:0]
INPUT_FIFO input fiber 9/8	0x40	bit[31:16]/[15:0]
INPUT_FIFO input fiber 11/10	0x50	bit[31:16]/[15:0]
INPUT_FIFO input fiber 13/12	0x60	bit[31:16]/[15:0]
INPUT_FIFO input fiber 15/14	0x70	bit[31:16]/[15:0]
INPUT_FIFO outputt fiber 1/0	0x80	bit[31:16]/[15:0]
INPUT_FIFO output fiber 3/2	0x90	bit[31:16]/[15:0]
INPUT_FIFO output fiber 5/4	0xA0	bit[31:16]/[15:0]
INPUT_FIFO output fiber 7/6	0xB0	bit[31:16]/[15:0]
INPUT_FIFO output fiber 9/8	0xC0	bit[31:16]/[15:0]
INPUT_FIFO output fiber 11/10	0xD0	bit[31:16]/[15:0]
INPUT_FIFO output fiber 13/12	0xE0	bit[31:16]/[15:0]
INPUT_FIFO output fiber 15/14	0xF0	bit[31:16]/[15:0]
DUMP_FIFO output fiber 1/0	0x88	bit[31:16]/[15:0]
DUMP_FIFO output fiber 3/2	0x98	bit[31:16]/[15:0]
DUMP_FIFO output fiber 5/4	0xA8	bit[31:16]/[15:0]
DUMP_FIFO output fiber 7/6	0xB8	bit[31:16]/[15:0]
DUMP_FIFO output fiber 9/8	0xC8	bit[31:16]/[15:0]
DUMP_FIFO output fiber 11/10	0xD8	bit[31:16]/[15:0]
DUMP_FIFO output fiber 13/12	0xE8	bit[31:16]/[15:0]
DUMP_FIFO output fiber 15/14	0xF8	bit[31:16]/[15:0]

Table 4: Virtex 5 Data Spy Registers.

Name	VME Addr	Bit Assignment
LENGTH_FIFO output fiber 1/0	0x100	bit[27:16]/[11:0]
LENGTH_FIFO output fiber 3/2	0x110	bit[27:16]/[11:0]
LENGTH_FIFO output fiber 5/4	0x120	bit[27:16]/[11:0]
LENGTH_FIFO output fiber 7/6	0x130	bit[27:16]/[11:0]
LENGTH_FIFO output fiber 9/8	0x140	bit[27:16]/[11:0]
LENGTH_FIFO output fiber 11/10	0x150	bit[27:16]/[11:0]
LENGTH_FIFO output fiber 13/12	0x160	bit[27:16]/[11:0]
LENGTH_FIFO output fiber 15/14	0x170	bit[27:16]/[11:0]
COE_HEADER_FIFO output fiber 0	0x104	bit[13:0]
COE_HEADER_FIFO output fiber 1	0x114	bit[13:0]
COE_HEADER_FIFO output fiber 2	0x124	bit[13:0]
COE_HEADER_FIFO output fiber 3	0x134	bit[13:0]
COE_HEADER_FIFO output fiber 4	0x144	bit[13:0]
COE_HEADER_FIFO output fiber 5	0x154	bit[13:0]
COE_HEADER_FIFO output fiber 6	0x164	bit[13:0]
COE_HEADER_FIFO output fiber 7	0x174	bit[13:0]
COE_HEADER_FIFO output fiber 8	0x184	bit[13:0]
COE_HEADER_FIFO output fiber 9	0x194	bit[13:0]
COE_HEADER_FIFO output fiber 10	0x1A4	bit[13:0]
COE_HEADER_FIFO output fiber 11	0x1B4	bit[13:0]
COE_HEADER_FIFO output fiber 12	0x1C4	bit[13:0]
COE_HEADER_FIFO output fiber 13	0x1D4	bit[13:0]
COE_HEADER_FIFO output fiber 14	0x1E4	bit[13:0]
COE_HEADER_FIFO output fiber 15	0x1F4	bit[13:0]

Table 5: Virtex 5 Data Spy Registers - continued

3 Status Registers

These RO registers are used for reading the status of various signals inside the FRONTEND module plus other miscellaneous monitoring signals, including counters and the status of the MUX module.

Table 6: Frontend Module FIFOs status register. For single bit definition see Table 7. Normal status for masked inputs is 0x55. Any deviation will indicate a problem.

Name	VME Addr	Bit Assignment
fiber 0 FIFOs status	0x04	bit[7:0]
fiber 1 FIFOs status	0x04	bit[15:8]
fiber 2 FIFOs status	0x04	bit[23:16]
fiber 3 FIFOs status	0x04	bit[31:24]
fiber 4 FIFOs status	0x14	bit[7:0]
fiber 5 FIFOs status	0x14	bit[15:8]
fiber 6 FIFOs status	0x14	bit[23:16]
fiber 7 FIFOs status	0x14	bit[31:24]
fiber 8 FIFOs status	0x24	bit[7:0]
fiber 9 FIFOs status	0x24	bit[15:8]
fiber 10 FIFOs status	0x24	bit[23:16]
fiber 11 FIFOs status	0x24	bit[31:24]
fiber 12 FIFOs status	0x34	bit[7:0]
fiber 13 FIFOs status	0x34	bit[15:8]
fiber 14 FIFOs status	0x34	bit[23:16]
fiber 15 FIFOs status	0x34	bit[31:24]

Table 7: FIFO Status Register bitmap.

Bit	Definition
7	Length FIFO full
6	Length FIFO empty
5	COE Header fifo full
4	COE Header fifo empty
3	Dump fifo full
2	Dump fifo progr empty (< 4 words)
1	Input fifo full
0	Input fifo empty

Table 8: Counters of packet IN and OUT of Input FIFO and current number of packets in INPUT_FIFO. Each counter is 8-bit and four counters are packed in a single 32-bit VME word starting from the LSB fiber.

fiber 0 thru 3 packet IN count	0x44	bit[31:0]
fiber 4 thru 7 packet IN count	0x54	bit[31:0]
fiber 8 thru 11 packet IN count	0x64	bit[31:0]
fiber 12 thru 15 packet IN count	0x74	bit[31:0]
fiber 0 thru 3 packet OUT count	0x84	bit[31:0]
fiber 4 thru 7 packet OUT count	0x94	bit[31:0]
fiber 8 thru 11 packet OUT count	0xA4	bit[31:0]
fiber 12 thru 15 packet OUT count	0xB4	bit[31:0]
fiber 0 thru 3 PACKET_TO_COME count	0xC4	bit[31:0]
fiber 4 thru 7 PACKET_TO_COME count	0xD4	bit[31:0]
fiber 8 thru 11 PACKET_TO_COME count	0xE4	bit[31:0]
fiber 12 thru 15 PACKET_TO_COME count	0xF4	bit[31:0]
WR_DATA_COUNT fiber 1/0	0x180	bit[28:16]/[12:0]
WR_DATA_COUNT fiber 3/2	0x190	bit[28:16]/[12:0]
WR_DATA_COUNT fiber 5/4	0x1A0	bit[28:16]/[12:0]
WR_DATA_COUNT fiber 7/6	0x1B0	bit[28:16]/[12:0]
WR_DATA_COUNT fiber 9/8	0x1C0	bit[28:16]/[12:0]
WR_DATA_COUNT fiber 11/10	0x1D0	bit[28:16]/[12:0]
WR_DATA_COUNT fiber 13/12	0x1E0	bit[28:16]/[12:0]
WR_DATA_COUNT fiber 15/14	0x1F0	bit[28:16]/[12:0]

In normal running conditions, counts of packet IN and OUT should be the same. The number of PACKET_TO_COME is the output of a UP_DOWN counter, counting UP every L1A and down every time a full packet (i.e. a number of word equal to the packet LENGTH) sit the INPUT FIFO. For 64 sampling triggers, the maximum number of packets that can fit in the input buffer at any given time is 7. The value of PACKET_TO_COME is used in the logic to predict whether the INPUT_FIFO is getting full:

$$\text{PACKET\_TO\_COME} \times \text{MAX\_WORD} < \text{0x1FFF - WR\_DATA\_COUNT}$$

where MAX_WORD is the maximum ADC packet size, 0x1FFF is the INPUT_FIFO size, and WR_DATA_COUNT is the number of word already written to the INPUT_FIFO, all in units of in 16-bit word.

Name	VME Addr	Bit Assignment
Current fiber number processed in MUX	0x08	bit[3:0]
Current trigger number processed in MUX +1	0x08	bit[21:4]
L2R counter	0x18	bit[15:0]
L2A counter	0x18	bit[31:16]
L1A counter	0x28	bit[15:0]
DUMP Ready counter	0x28	bit[31:16]
errors bit fiber 0 thru $7^{(\circ)}$	0x38	bit[31:0]
errors bit fiber 8 thru $15^{(\circ)}$	0x48	bit[31:0]
single input i fiber issued L1a_disable$^{(*)}$	0x58	bit[i]
single input i COE DUMP_DONE issued wo TRIGGER_DONE (or L2R_TRIGGER_DONE)	0x58	bit[$i+16$]
L2R_Trigger_done counter	0x68	bit[15:0]
Trigger_done counter	0x68	bit[31:16]
L2_request counter (5 per trigger)	0x78	bit[31:0]
more errors bit fiber 0 thru $7^{(\circ)}$	0x1E4	bit[31:0]
more errors bit fiber 8 thru $15^{(\circ)}$	0x1F4	bit[31:0]

Table 9: Virtex 5 miscellaneous status and counters. All counters are clear at the start of a SPILL, unless specified. For the details of the error bits, see Table10. ($^\circ$) 4-bits per fiber, starting from LSB fiber.(*) This register is cleared only by a fifo reset.

Table 10: Single Bit Error: these are set inside the INPUT_MANAGER or COE_MANAGER modules and are stay high even if the error condition disappears until the next LIVE.

Bit	Definition
7	IDLE word (after last COE word) is not 0x50BC or 0xC5BC
6	COE word does not have bit(15,14)=(0,1)
5	Energy word does not have bit(15,14)=(1,0)
4	Header word does not have bit(15,14)=(1,1)
3	Input FIFO about to get full
2	Length Error in COE Manager: packet length less than 60 words
1	First valid word does not have bit(15,14)=(1,1)
0	Word not valid or with error during ADC packet transmission

4 FIFO Registers

These registers read the internal content of different FIFOs inside the FROTEND module. They can be readout via DMA (direct memory access). To read out the FIFO via VME use the command:

./vme7700_dma *read* "slot number" *1X00000 depth*

where *depth* is specified in Table 11.

Name	VME Access	VME Addr	Depth
INPUT_FIFO fiber 0	RO	0x1000000	8k
INPUT_FIFO fiber 1	RO	0x1100000	8k
INPUT_FIFO fiber 2	RO	0x1200000	8k
INPUT_FIFO fiber 3	RO	0x1300000	8k
DUMP_FIFO fiber 0	RO	0x1400000	2k
DUMP_FIFO fiber 1	RO	0x1500000	2k
DUMP_FIFO fiber 2	RO	0x1600000	2k
DUMP_FIFO fiber 3	RO	0x1700000	2k
LENGTH_FIFO fiber 0	RO	0x1800000	64
LENGTH_FIFO fiber 1	RO	0x1900000	64
LENGTH_FIFO fiber 2	RO	0x1A00000	64
LENGTH_FIFO fiber 3	RO	0x1B00000	64
COE_FIFO fiber 0	RO	0x1C00000	1K
COE_FIFO fiber 1	RO	0x1D00000	1K
COE_FIFO fiber 2	RO	0x1E00000	1K
COE_FIFO fiber 3	RO	0x1F00000	1K

Table 11: Bulk Registers Bitfields.