K0TO Note XXX
Version 10.0
May 6, 2016

MACTRIS+ Board VME Address Space for June 2016 Run

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This document specifies the VME Address Space defined in the firmware of the new MAster Control and TRIgger Supervisor (MACTRIS+) board. This board is meant to take over the functionality of the L1 Master MACTRIS and be installed in slot 12 of the L1 Trigger Crate. On top of reproducing all of the functionality of the previous MACTRIS (system clock generation, LIVE and L1A decision), this board has some extra features: ability to distribute clock and DAQ control signals to up to four VME crates via Slave Mactris; ability to exchange signals via two 2.5Gbs fibers; ability to receive and send signals directly to COE MActris in slot 12 of the L2 Trigger Crate; ability to store data in local DDR3 4Gb memory and to read it out via Ethernet port.

The new Mactris will be used during the 2016 June run, for which the KOTO DAQ will be upgraded to include the readout of the newly installed Inner Barrel (IB) detector. With the addition of this new veto detector, we have to add a third trigger crate, the Veto Trigger Crate, which will house all of the L1 Veto Trigger boards. We will also add an MT board to the DAQ, which will receive the veto and detector status bits used in the L1A decision from Mactris via the L1 fiber, and will be read out using the standard readout path after the L2A has been made. Finally, we plan to save the veto and detector status bits for each "raw" L1A, either on the external DDR3 memory or on the internal FPGA memory, and read this info out at the end of each spill via a 1Gb connection to banjo-1.

The MACTRIS+ board has a XC7A200 Artix 7 FPGA and its firmware has been developed completely in Verilog using the Vivado design platform. The MACTRIS+ firmware developed for the KOTO June 2016 run is version 4.5 and above. It is compatible with version 4.0 and above of the COE Mactris firmware, version 5.5 and above of the L1Trigger Virtex5 firmware, version 2.6.C and above of the L2 Trigger Virtex 5 firmware and version A.8 and above of the L2 Trigger Virtex 4 firmware.

As it was for the previous Master MACTRIS board, the MACTRIS+ is designed to make a L1A decision using all of the veto detectors plus the total energy measured in the CsI calorimeter. It assumes that up to 12 independent L1 Veto decisions are coming in via bit(23:18) of the left and right P3 Daisy-chain signals, while bit(17:0) of both chains are reserved for the calorimeter total sum. A signal monitoring the status of the TLK errors in the L1 Trigger boards is received via the Slave Mactris in the L1 trigger crate. Signals flagging the status of the L2 input buffer and 2Gb on-board memories, as well as ??, are received via the Slave Mactris in the L2 Trigger crate. Signals controlling the L2 Accept decision are exchange between the Mactris+ and the COE Mactris via a dedicated RJ45 connector.

Section 1 gives an overall description of the main features of the Mactris board. Section 3 lists the L1 Master MACTRIS control registers (Tables 4, 5, 6 and 7) and monitoring registers (Table 8 and 9). Section 4 lists the signals coming in via the P2 and P3 backplane pins. Section 5 describes the content of the FIFOs instantiated inside the Master MACTRIS FPGA. Section 6 summarizes the VME registers defined for the SMACTRIS firmware. Finally Section 7 give a sheet-by-sheet description of the contents of the FPGA firmware.

1 The MACTRIS Board

The MACTRIS+ board, see Figure **??**, is a 9U-tall VME board designed to control the KOTO DAQ. The board has multiple front panel connectors, described here from top to bottom: four high-density double-deck 68-pin SCSI connectors (AI, BI, CI and DI) designed to exchange DAQ Control signals with up to four trigger crates (when looked from the front of the board, AI and CI are on the left-side, and BI and DI are on the right-side); two LC optical-fiber connectors (J10 and J11); two LEMO connectors (J4 and J5), receiving beam synchronization signals from the accelerator; four RJ45 connectors, used for communication with the COE board (J6), the ADC Control port (J7), external trigger sources (J2) and the Master Fanout (J1) control port; one 12-pin JTAG connector used for the PROM and FPGA programming; and a 1 Gb Ethernet port. The back of the board has standard P0, P1 and P2 connectors compatible with the specifications of the CDF VME64P 9U crates [1], plus a P3 connector which plugs into a custom-designed backplane.

The Master MACTRIS drives equal copies of the DAQ Controls, consisting of 34 differential signals, to each of the Slave MACTRIS in the L1 Trigger, L1 Veto and L2 Trigger crates. Each of the Slave Mactris in those crates receives these signals via the CHIE port and routes them to the P2 backplane. Note that unlike with the old Master MACTRIS board, these signals are not passed via flat ribbon cable but but via a bundled cable designed for high speed signals out of the high-density SCSI connector. As a result, on the Slave Mactris side, an adaptor board is needed to go from the old to the new style connector. The majority of this signals are driven by Mactris+ but 5 are Open Collector signals reserved for communication from the trigger crate to Mactris+. Table 1 lists which signals are connected for each trigger crate.

The J1 RJ45 connector has 3 LVDS output and 1 LVDS input and is used to drive the ADC Control signals (clock, Live, L1A and Error) from MACTRIS+ to the Master Fanout board, which in turn takes care of distributing these signals to all of the ADCs in the system [2]. The J2 RJ45 connector has two LVDS inputs and two LVDS outputs signals and can receive/drive signals from external sources, such as the LED calibration system and the beam monitor system. It can be interfaced to NIM signals by using the "NIM to LVDS Board" which translates between electrical levels. The J6 RJ45 connector is a mirror copy of J2, with two LVDS outputs and two LVDS inputs signals. It receives from COE MACTRIS the L2A_R signal, who length (16 vs 4 clks) encodes whether the trigger has resulted in a L2A vs L2R, and the COE protocol request signal, which is sent to the L2 trigger boards when the next COE sum is to be sent down

[1] For details, see the "The K0T0 Trigger Crate VME Backplane" KOTO note, Monica Tecchio, Mar, 31, 2011.

[2] The Master Fanout boards drives 32 copies of the ADC Control Signals to the Slave Fanout boards, which in turn multiply them by 16 and distributes them to each ADC board in a front-end crate. The Fanout boards are housed a 9U Fanout crate situated close to the ADC frontend crates

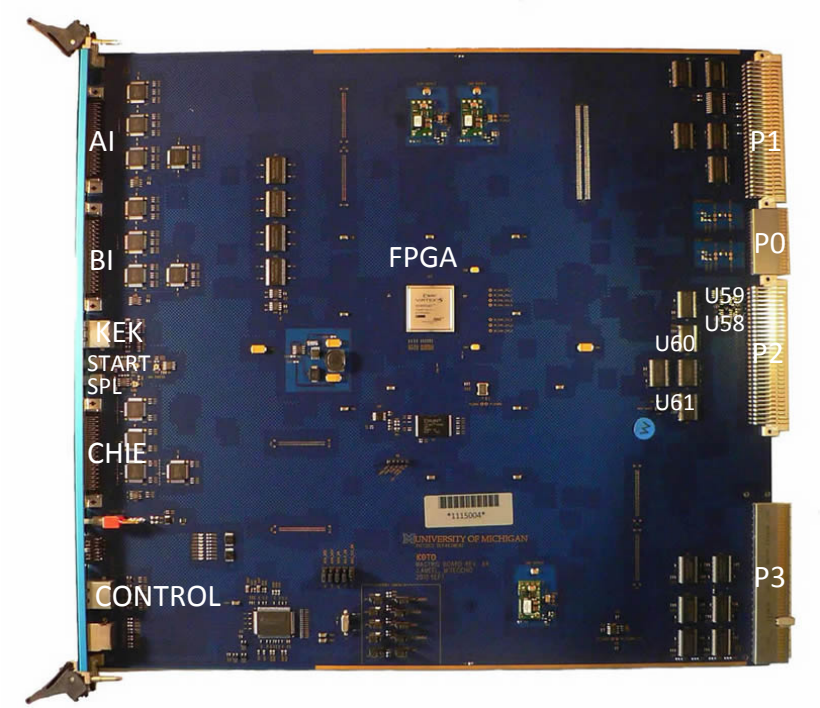

Figure 1: Picture of the MACTRIS+ board showing the most relevant features.

the P3 daisy-chain [3] In return in sends to COE MACTRIS the acknowledge of the COE sum request, as well as the "early" L1A signal. The J7 RJ45 connector is a copy of J1 and unused at the time of this document. Finally, the J4 lemo connector receives the BEAM_START, a NIM pulse at start of beam injection in the machine, while J5 receives BEAM_SPILL, a NIM gate for duration of proton spill.

The P3 backplane is a custom-designed backplane connecting signal across all slots except slot 1. In particular slots 4,5,6, 9,10,11, 13,14,15 and 18,19,20 have access to 24 lines which are connected in a daisy-chain fashion and are reserved for trigger boards receiving signals from the CsI detector. Slots to the right and to the left of slot 12 form two separate daisy-chains, starting at slot 4 and slot 20 and ending at slot 12, which in the following will be referred as Left and Right Daisy-Chain. Every slot in the daisy-chain has also access to two point-to-point (PTP) lines connecting the single slot directly to slot 12. Finally, every slot in the crate, i.e. not only the slots in the daisy-chains, have access to two bussed lines running along the whole backplane length. These provide the only connections to MACTRIS for boards receiving signals from veto detectors.

[3]The COE calculation requires 5 separate sums to be calculated for the whole calorimeter: ΣE_T, 2 partial $\Sigma E \cdot x$ and two partial $\Sigma E \cdot y$.

Trigger Crate	from MACTRIS+	to MACTRIS+	descrition
All	CLK		8 ns system clock
All	LIVE		Spill gate
All	L1A		L1 Accept decision
L1		KOTO_ERROR	TLK error observed
L2	L2A_EN		L2 decision acknowledge
L2	L2A		L2 Accept/Reject decision
L2		KOTO_FULL	input buffer full decision
L2		KOTO_ERROR	L2 memory full decision
L2		KOTO_NOT_DONE	input buffer overflow
L2	KOTO_RSVD		COE sum request
L2		KOTO_OC_RSVD	COE sum acknowledge

Table 1: DAQ Control signals used by for the different trigger crates: if "All", those signals are sent to every trigger crate. The signals "to MACTRIS+" are negative logic Open Collector signals which can be issues, or pulled low, by ANY slot in the crate. The TLK error signal is issued when at least 32 TLK errors are observed in a given board. The L2 accept (L2A) or reject (L2R) is decided by L2A being high or low when L2A_EN is seen. The input buffer full decision is based on the number of L1A triggers which have not yet left the input FIFO, while the input buffer overflow indicated that the input FIFO is full. The COE sum protocol is based on a request to send the next of the five COE sums to the P3 and the acknowledge from each board that the sum has been sent.

2 January 2016 Run L1A Trigger Logic

For the June 2016 KOTO run, the L1A decision is generate by a combination of calorimeter, veto and external trigger signals. The presence of the LIVE signal is a pre-requisite for the L1A decision. LIVE is an approximately 4s long gate started by a pulse coming via the J4 input and signaling the start of the proton spill. The proton spill itself lasts only for 2s, with a repetition time of 6s. The last two seconds of LIVE are used to collect calibration and cosmic triggers. The actual length of the proton spill is measured by the J5 signal, which is a straight copy of the SPL NIM input. Figure 2 show a schematic view of the logic used inside the firmware to generate the LIVE signal, which is broadcast to the rest of the DAQ.

The CsI energy trigger is generated by requiring the total energy deposited in the calorimeter to be above a programmable threshold and use this condition as an enable to the energy peak finding logic. The energy peak finding logic is simply tagging the first 8 ns sample above threshold for which the energy is not larger than the previous sample. Two separate calorimeter triggers to be used in the final L1A decision are issued: a total energy sum above a "low" threshold (SUM_PEAK) and a total energy sum above a "high" threshold (SUM_PEAK1).

The Master MACTRIS firmware is also designed to receive the crate-sum (CSUM) trigger decision from each L1 Trigger board using one of the P3 backplane point-to-point signal (PTP_1). The CSUM trigger is fired when the peak of the total energy sum for a single L1 Trigger board, which corresponds to the total energy of a single ADC crate, is found. Using these 12 separate "regional" trigger decision, Master MACTRIS generates two more inputs

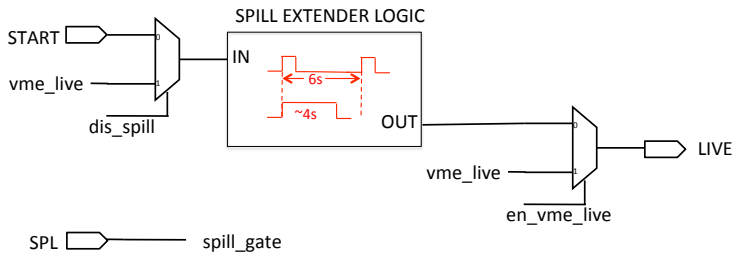

Figure 2: LIVE and SPILL_GATE logic: for May 2013 run, the START signal has a repetition rate of 6s.

(CSUM_GATE and CSUM_GATE1) to the final L1A decision. These decision are generated by requiring a minimum number of regional triggers above two separate thresholds.

Up to 12 L1 Veto bits are allowed into the the final L1 Trigger accept (L1A) decision. This is achieved by installing two L1 Trigger boards with a dedicated firmware, called Master L1 Veto boards, in the outermost slots of the left (slot 4) and right (slot 20) daisy-chain of the L1 Trigger crate. Each of these boards drives 18 of the 24 daisy-chain lines with the partial calorimeter energy sum and the remaining 6 lines with the L1 veto decisions. The input fibers to these Master L1 Veto boards are connected to eight L1 Veto boards (inputs 0 thru 7) and eight CsI ADC boards (inputs 8 thru 15). The mapping of Veto detectors to input fibers and P3 backplane signal is described in Table 1. The logic for the final L1 veto decision within a given detector is programmed inside the Master L1 Veto board firmware and specified in the L1 Trigger board VME Address space document. These twelve L1 veto signals (6 from each daisy-chain) are time aligned to each other and to the Csi calorimeter trigger decisions inside MACTRIS, and made into gates of programmable width (VETO_BIT[11:0]) before being used in coincidence or anti-coincidence with the CsI energy trigger to make the final L1A final decision.

Other inputs to the L1A decision not coming from the CsI or veto detectors are provided by two external trigger signals (EXT_BEAM1_TRG and EXT_BEAM2_TRG) connected to the L1 Master MACTRIS via the KEK RJ45 front-panel connector. For the May 2013 run, the EXT_BEAM1_TRG was the logical OR of the CLOCK, LED, LASER and COSMIC triggers, where the CLOCK and LED triggers were set to run at a constant rate of 10 Hz while the LASER trigger was set at 5 Hz. While CLOCK was driven by a programmable NIM generator module, the LED and LASER were signals were used to generate light flashes to their respective optical devices upon which the Csi energy trigger was fired. Finally the COSMIC trigger is made by a coincidence of scintillator counters places around the vacuum chamber.The EXT_BEAM2_TRG was driven by TMOM, a monitoring random signal generated by the accelerator, which is received by a NIM module in the counting room and prescaled before forcing a L1A trigger decision. While the first external trigger is used mainly for calibration purposes, the second external trigger is used to monitor the effect of accidentals in our detector.

In the following, details of the implementation of the L1A trigger inside the Master MACTRIS firmware are presented. A pictorial schematic view of the logic is shown in Figure 3. The SUM_PEAK, LEFT_RIGHT_GATE, CSUM_GATE and VETO_GATE(11:0) trigger signals are

Veto Detector	Input Fiber	Daisy-Chain Bit	Input Fiber Driver
CV	Left Master input 0	Left bit(18)	L1 Veto slot 3
FB/MB	Left Master input 1	Left bit(19)/(21)	L1 Veto slot 7
NCC	Left Master input 2	Left bit(20)	L1 Veto slot 8
OEV	Left Master input 3	Left bit(22)	L1 Veto slot 16
Laser ADC	Left Master input 4	Left bit(23)	ADC12, slot 16
MB Cosmic ADC	Left Master input 5	Left bit(23)	ADC12, slot 17
FB/CsI Cosmic ADC	Left Master input 6	Left bit(23)	ADC12, slot 18
CC03/4/5/6	Right Master input 0	Right bit(18/19/20/21)	L1 Veto slot 21
BHCV/BHPV	Right Master input 1	Right bit(22/23)	L1 Veto slot 17

Table 2: Mapping of Master L1 Veto input fibers to Daisy-Chain bits. Left Master input fibers 7 and Right Master input fibers 2 thru 7 are unused in the May 2013 run. The last column reports either the crate and slot number of the ADC board driving directly the Master Veto input fiber or the slot number in the L1 trigger crate of the Slave L1 Veto board whose output fiber 7 drives the Master Veto input fiber.

used to generate an internal `L1_trigger` decision, which seeds a raw `trigger` after the two external trigger signals are included. This raw trigger is the basis for the final `l1a_trigger` signal which is broadcast to all of the ADC and Trigger boards in the system. The final L1A trigger is either a 3-clk or 5-clk long pulse generated by the L1A_MANAGER block: the shorter length signals physics triggers, for which the COE cut has to be applied by the L2 Trigger; the longer length is reserved for minimum bias and other calibration triggers for which we want an automatic L2 accept.

The internal `L1_trigger` is the OR of 8 independent trigger decisions, each generated inside the YASU_TRIGGER_LOGIC block (see Figure 4). By setting 18 programmable masks, the output of this block can be one of the following combinations: a calorimeter-only trigger[4], a veto-only trigger [5], the coincidence of a calorimeter and veto trigger, or the anti-coincidence of a calorimeter and veto trigger. The last combination is what used for physics and normalization triggers while the others are used for special calibration and min. bias triggers. Note how any of the YASU_TRIGGER_LOGIC outputs can be individually disabled for the duration of the SPILL_GATE signal. As a result some calibration triggers are allowed only when the proton spill is terminated (off spill) but the LIVE signal is still high. Another knob that can be independently dialed for each output is a pre scale factor so that we can control the relative rate of each trigger. Table 3 reports the inputs and the logic used for typical triggers used in the May run and their respective pre-scale factors for a run at 24kW beam power.

The internal trigger decision can be disabled when the firmware detects a LOSS_OF_SYNC condition, that is when the TLK errors have reached a maximum count. For diagnostic purposes, it can also be bypassed altogether when either the external triggers or the VME simulated L1A signals are used in generating the L1A decision. If none of this special conditions is set, the OR of the L1_ trigger, EXT_BEAM1_TRG and EXT_BEAM2_TRG is sent

[4]A calorimeter trigger can be the coincidence of any SUM_PEAK, SUM_PEAK1, CSUM_GATE and CSUM_GATE1 triggers when appropriately enabled.

[5]A veto trigger can be either the OR or the AND of any enabled veto gates, see comment (p).

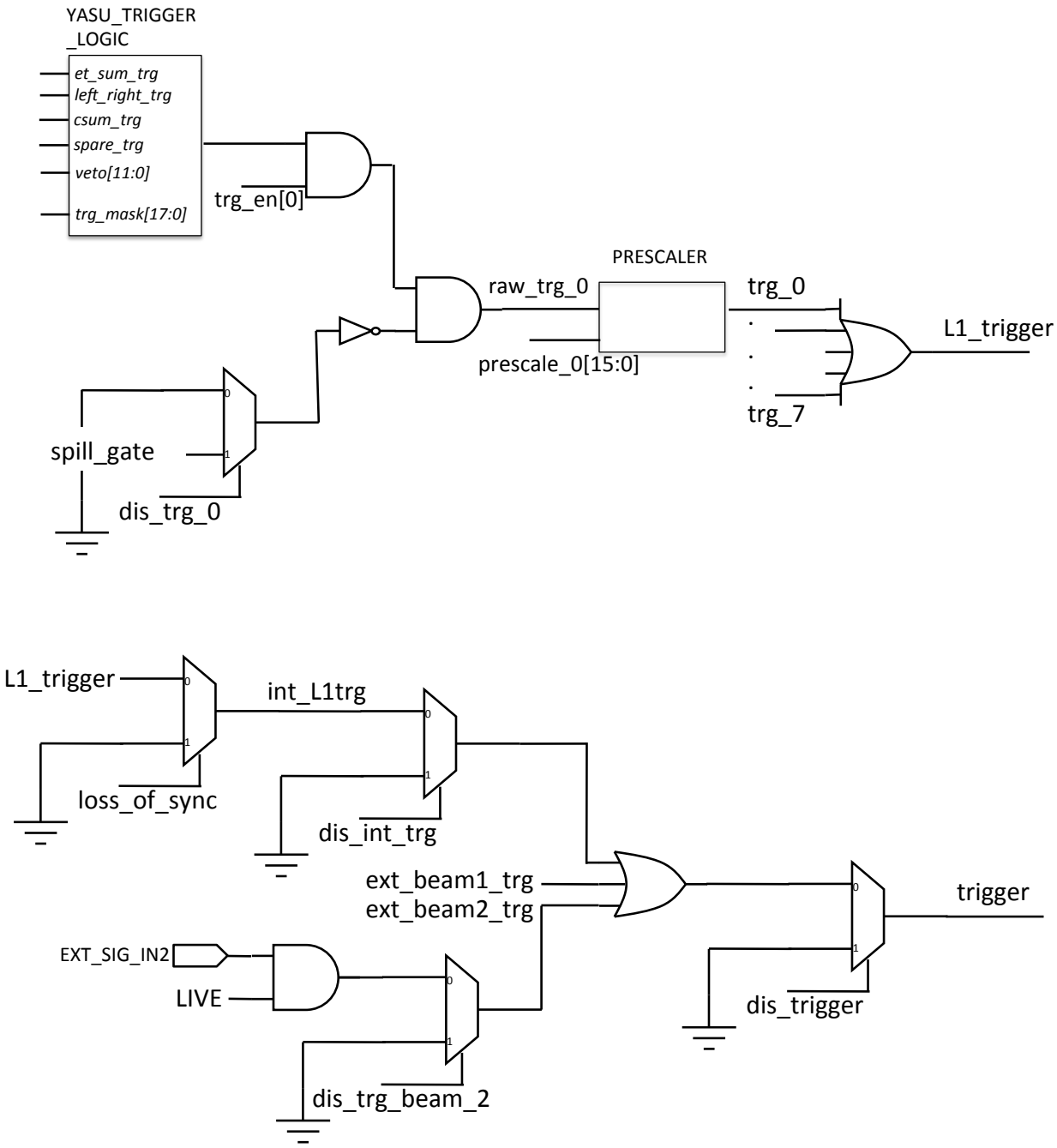

Figure 3: Details of the L1 trigger decision logic implementation: the top diagram show the 8-input OR gate used for the internal `L1_trigger` signal. All of the inputs to the OR gate are generated by the same logic as the one esplicitly shown for `trg_0`. The bottom diagram shows the logic used in generating the raw `trigger` signal sent to the L1A_MANAGER block. The EXT_BEAM1_TRG signal is generated by a chain analogous to what producing EXT_BEAM2_TRG but driven by the EXT_SIG_IN1 LVDS input. See Table 5 for a list of the specific bits driving the different disables signals.

Trigger	Logic	Prescale
Physics	(Total_CsI & $\overline{VETO}$ & COE cut	1
Normalization	(Total_CsI & $\overline{VETO}$	30
Minimum Bias	Total_CsI	300
Calibration	Total_CsI & CS1& $\overline{VETO}$	10
NCC Calibration	NCC Offspill Only	1
OEV Calibration	OEV Offspill Only	1
CsI Calibration	Total_CsI Offspill Only	1
Ext. Trigger 1	CLOCK & LASER & LED	1
Ext. Trigger 2	TMON	1

Table 3: Typical trigger table for a May 2013 run at 24kW beam power: Total_Csi means SUM_PEAK > 500 MeV; VETO means the OR of CV, NCC, MB and CC03 triggers; and CS1 means at least one CSUM trigger reported. External Triggers are added to the internal trigger obtained as the OR of the first 7 triggers . As a reminder, the inclusion/exclusion of the COE cut (COE>165 cm) is encoded in the length of the final L1A trigger decision.

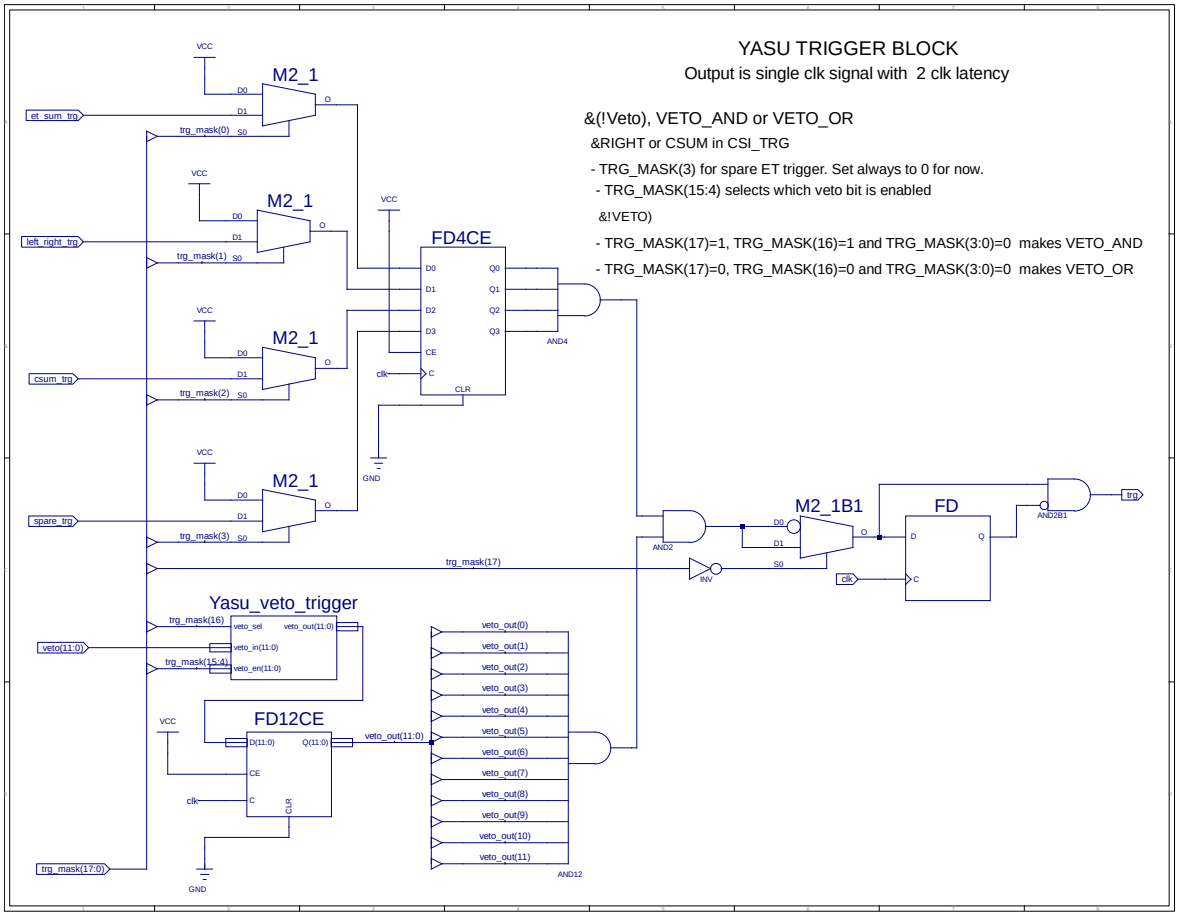

Figure 4: Details of the YASU_TRIGGER_BLOCK.

to the L1A_MANAGER block. This block masks consecutive L1 trigger requests if there are less than 4-clk cycle apart, shapes the L1A into a 3 or 5-clk long pulse as instructed by the L2A_MANAGER block [6] and delays the decision before sending it out to the ADC boards so it coincides with the time the digitized energies are about to fell off the 512-clk deep pipeline. This block also disables the assertion of L1As for the remaining duration of the spill when their number has reached a maximum value (typically the maximum number of triggers which can fit in the 2Gb memories). This condition has to be actively cleared before the next LIVE by issuing L1A_MAX count reset. A second not permanent L1A disable condition is generated in situations of very high instantaneous trigger rates when multiple consecutive events risk to fill the L2 input buffers. This INPUT_FIFO_FULL decision is taken inside the L2 Trigger Virtex5 firmware independently by each of the 8K deep FIFOs receiving the packets sent by the ADC in response to a L1A trigger via the L2 input fibers. These 8K buffers are meant to store the ADC packets while the total COE information is calculated for a particular event so that a L2 decision can be made. Upon a L2 accept (L2A) decision, the packets are read from all input buffers and saved onto the 2GB memories.

The INPUT_FIFO_FULL decision is made comparing the number of words not already written into a given input FIFO with the number of words still to come given the total number of triggers read out from the buffer and the total number of L1A issued. For this comparison, the size of the single trigger is taken to be the size of an uncompressed event with 64 samplings. Let's remind the reader that up to 7 triggers can fit inside the input FIFO is no compression is done. The INPUT_FIFO_FULL signal is combined the L2_MEMORY_FULL signal which inform Master MACTRIS that at least one L2 Trigger board has its 2 Gb memory full. The L2_MEMORY_FULL decision is based on the number of addresses written to memory for a given spill reaching a value of 0xFE0_0000, which corresponds the the absolute maximum value of bytes that can fit in the memory (2Gb/8bit = 0x1000_0000) minus a 16 times the total storage of the input FIFOs in units of bytes (16 x 16 FIFO x 16K = 0x40_0000). Figure 5 shows a cartoon of the logic used to generate the L1A disable decision based on the two sign as described above.

Additional features implemented inside the firmware as part of the trigger logic include: independent programmable delays for each of the CSI triggers and veto bits; programmable prescales for each input of the `L1_trigger` decision; scalers for each input signal used in the trigger decision; and counters for the relative delay of trigger inputs with respect to LIVE.

3 Master MACTRIS VME Registers

(a) The daisy-chain calibration measures the time of the first non-zero Right and Left daisy-chain signal reaching MACTRIS after LIVE is issued. This register reads these delays, in units of 8 ns clock ticks, using bits(7:0) and bits(23:16) for the Left and Right daisy-chain, respectively. To measure this delay, input data from the left and right daisy chain have to be enabled by setting bit(16) and bit(17) of register 0xcc, respectively, to 1. Their default value is 1.

(b) This register can simulate LIVE on/off by writing 1/0 to bit(0) of register 0x1c. If bit(4) of

[6] See comment (i).

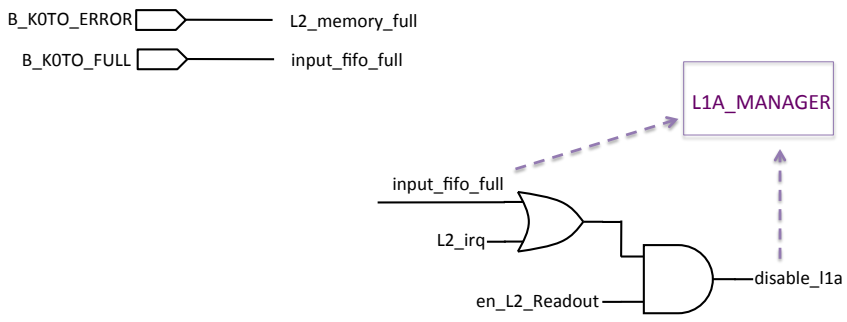

Figure 5: Details of the implementation of the L1A_DISABLE decision inside the Master MACTRIS firmware.

VME Command Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read daisy-chain calibration$^{(a)}$	16	R0	0xc	data[23:16,7:0]
Simulate LIVE to ADCs$^{(b)}$	1	WO	0x1c	data[0]
Set daisy-chain delays$^{(c)}$	14	RW	0x2c	data[23:16,7:0]
Simulate L1A to ADCs$^{(d)}$	1	WO	0x3c	data[0]
Counters Reset$^{(n)}$	1	WO	0x4c	data[0]
Set L1A delay$^{(e)}$	9	RW	0x5c	data[8:0]
Set LIVE gate length$^{(f)}$	30	RW	0x6c	data[29:0]
Set Sum Energy "Low" Threshold$^{(g)}$	18	RW	0x7c	data[17:0]
Set Sum Energy "High" Threshold$^{(g)}$	14	RW	0x7c	data[31:18]
Set Left Energy Threshold$^{(g)}$	18	RW	0x9c	data[17:0]
Reset L1A_MAX Count$^{(h)}$	1	WO	0xac	data[0]
Set Right Energy Threshold$^{(g)}$	18	RW	0xbc	data[17:0]
Enables/Disables (see Table 5)	24	RW	0xcc	data[31:0]
FIFOs Reset$^{(n)}$	1	WO	0xdc	data[0]
Status Bits (see Table 6)	32	RO	0xec	data[31:0]
Firmware VME Reset$^{(n)}$	1	WO	0xfc	data[0]

Table 4: List of commands defined for the Master MACTRIS Board via VME registers 0xYC, where Y=0 thru F.

VME Enable Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Disable Trigger 0 during SPILL_GATE	1	RW	0xcc	data[0]
Disable External Beam Trigger 1	1	RW	0xcc	data[1]
Disable External Beam Trigger 2	1	RW	0xcc	data[2]
Disable ADC Error input$^{(q)}$	1	RW	0xcc	data[3]
Disable External LIVE$^{(b)}$	1	RW	0xcc	data[4]
Disable Trigger 1 during SPILL_GATE	1	RW	0xcc	data[5]
Disable Internal L1 Trigger$^{(p)}$	1	RW	0xcc	data[6]
Disable Internal and External L1 Trigger$^{(p)}$	1	RW	0xcc	data[7]
Disable Trigger 2 during SPILL_GATE	1	RW	0xcc	data[8]
Disable Trigger 3 during SPILL_GATE	1	RW	0xcc	data[9]
Enable VME LIVE$^{(b)}$	1	RW	0xcc	data[10]
Simulate ERROR from ADC$^{(q)}$	1	RW	0xcc	data[11]
Disable Trigger 4 during SPILL_GATE	1	RW	0xcc	data[12]
Disable Trigger 5 during SPILL_GATE	1	RW	0xcc	data[13]
Disable Trigger 6 during SPILL_GATE	1	RW	0xcc	data[14]
Disable Trigger 7 during SPILL_GATE	1	RW	0xcc	data[15]
Enable Left daisy-chain into Adder$^{(a)}$	1	RW	0xcc	data[16]
Enable Right daisy-chain into Adder$^{(a)}$	1	RW	0xcc	data[17]
Enable override of L2A decision$^{(i)}$	1	RW	0xcc	data[19]
Enable VME automatic L2A decision$^{(i)}$	1	RW	0xcc	data[20]
Enable Daisy Chain Integrity test	1	RW	0xcc	data[24]
Enable Random Trigger$^{(j)}$	1	RW	0xcc	data[26]
Enable L2A$^{(o)}$	1	RW	0xcc	data[27]
Enable Loss of Sync$^{(k)}$	1	RW	0xcc	data[28]
Enable Multiple L1A Simulation$^{(l)}$	1	RW	0xcc	data[29]
Enable TLK Error Counter$^{(k)}$	1	RW	0xcc	data[30]
Enable L2 Readout$^{(m)}$	1	RW	0xcc	data[31]

Table 5: List of enables controlled by register 0xcc in the Master MACTRIS Board firmware. Upon downloading the firmware into the FPGA or sending a VME firmware reset, register 0xcc is set to a default value of 0x8013045E.

Status Register Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Status of LIVE$^{(b)}$	1	RO	0xec	data[0]
Status of L1A_MAX Count$^{(h)}$	1	RO	0xec	data[1]
Status of L1A Disable$^{(l)}$	1	RO	0xec	data[2]
Status of ADC Error$^{(q)}$	1	RO	0xec	data[3]
Status of INPUT_FIFO_FULL$^{(m)}$	1	RO	0xec	data[4]
Status of LOSS_OF_SYNC$^{(k)}$	1	RO	0xec	data[5]
Status of B_K0TO_FULL$^{(y)}$	1	RO	0xec	data[6]
Status of TLK error$^{(k)}$	1	RO	0xec	data[7]
Status of Enable L2 Override$^{(i)}$	1	RO	0xec	data[8]
Status of L2_IRQ$^{(m)}$	1	RO	0xec	data[9]
Status of L1_L2_ETSUM FIFO empty$^{(z)}$	1	RO	0xec	data[9]
Status of L1_L2_ETSUM FIFO full$^{(z)}$	1	RO	0xec	data[10]
Status of ETSUM FIFO empty$^{(z)}$	1	RO	0xec	data[11]
Status of ETSUM FIFO full$^{(z)}$	1	RO	0xec	data[12]
Board Flavor$^{(x)}$	4	RO	0xec	data[19:16]
Firmware Revision$^{(x)}$	4	RO	0xec	data[23:20]
Firmware Version$^{(x)}$	4	RO	0xec	data[27:24]
Board Type$^{(x)}$	4	RO	0xec	data[31:28]

Table 6: Content of Status Register bits for the Master MACTRIS Board.

register 0xcc is set 1, a single 4s long LIVE is simulated; if bit(10) of register 0xcc is set 1, LIVE will stay until it is manually turned off (see Figure **??** for details). The default value for bit(4) and bit(10) is 1, meaning that the control of LIVE via the external START NIM signals is disables. The status of the LIVE signal can be monitored via bit(0) of register 0xec.

(c) This register decides by how many clock ticks one input daisy chain should be delayed with respect to the other so that the 24 bits are aligned with respect to LIVE. Bits(6:0) set the delay for the Left daisy-chain and bits(22:16) the delay for the Right daisy-chain. These are relative delays, that is only the delay of the daisy-chain seeing first an energy different than zero, as per note (a), should be set. The amount of this delay is equal to the difference of the daisy-chain calibration results, as readout by register 0xc.

(d) This register simulates a trigger signal approximately 300 ns long by writing 1 to bit(0). If issued after setting the "Enable Multiple L1A Simulation", (bit(29) of register 0xcc) to 1, it starts a burst of triggers as described in note (l). If issued after setting the "Enable Random Trigger", (bit(26) of register 0xcc) to 1, it starts a set of consecutive random trigger as described in note (j).

(e) This register defines the delay between the shaped L1A trigger being generated inside MACTRIS and the time is it sent out to the ADCs. It is set so that the L1A arrives to the ADCs in time with the gaussian shaped pulse falling off the ADC pipeline. Upon

VME Register Name	Size	VME Access	VME Addr[31..0]	Bit Assignm
Set Trigger Inputs Enable Mask$^{(p)}$	8	RW	0x4	data[7:0]
Set Trigger Mask for automatic L2A$^{(i)}$	9	RW	0x14	data[8:0]
Set No. of Samplings in triggered event$^{(s)}$	4	RW	0x24	data[3:0]
Set delay for VETO bits 0 thru 3$^{(t)}$	5x4	RW	0x34	data[31:0]
Set delay for VETO bits 4 thru 7$^{(t)}$	5x4	RW	0x44	data[31:0]
Set delay for VETO bits 8 thru 11$^{(t)}$	5x4	RW	0x54	data[31:0]
Set delay for CsI Triggers$^{(u)}$	5x4	RW	0x64	data[31:0]
Set gate length for CSUM trigger$^{(v)}$	8x2	RW	0x74	data[31:0]
Set Prescale for L1A inputs 2-3$^{(w)}$	32	RW	0x84	data[31:0]
Set Prescale for L1A inputs 0-1$^{(w)}$	32	RW	0x94	data[31:0]
Set Number & Gap of multiple L1As$^{(l)}$	16	RW	0xa4	data[15:0]
Set Number TLK errors$^{(k)}$	16	RW	0xb4	data[15:0]
Set Random Trigger Rate$^{(j)}$	32	RW	0xc4	data[31:0]
Set L1A_MAX Count$^{(h)}$	8	RW	0xd4	data[7:0]
Simulate Left Daisy Chain bits	24	RW	0xe4	data[23:0]
Simulate Right Daisy Chain bits	24	RW	0xf4	data[23:0]
Set gate length for veto bits 0 thru 3$^{(v)}$	32	RW	0x104	data[31:0]
Set gate length for veto bits 4 thru 7$^{(v)}$	32	RW	0x114	data[31:0]
Set gate length for veto bits 8 thru 11$^{(v)}$	32	RW	0x124	data[31:0]
Set Enable Mask for CSUM triggers$^{(v)}$	12	RW	0x134	data[7:0]
Set Minimum Number of CSUM_GATE triggers$^{(v)}$	4	RW	0x144	data[3:0]
Set Minimum Number of CSUM_GATE1 triggers$^{(v)}$	4	RW	0x144	data[19:16
Set length of L2A and L2R signals$^{(r)}$	32	RW	0x154	data[31:0]
Set Prescale for L1A inputs 4-5$^{(w)}$	32	RW	0x164	data[31:0]
Set Prescale for L1A inputs 6-7$^{(w)}$	32	RW	0x174	data[31:0]
Set Trigger Mask for trigger block 0$^{(p)}$	18	RW	0x184	data[17:0]
Set Trigger Mask for trigger block 1$^{(p)}$	18	RW	0x194	data[17:0]
Set Trigger Mask for trigger block 2$^{(p)}$	18	RW	0x1A4	data[17:0]
Set Trigger Mask for trigger block 3$^{(p)}$	18	RW	0x1B4	data[17:0]
Set Trigger Mask for trigger block 4$^{(p)}$	18	RW	0x1C4	data[17:0]
Set Trigger Mask for trigger block 5$^{(p)}$	18	RW	0x1D4	data[17:0]
Set Trigger Mask for trigger block 6$^{(p)}$	18	RW	0x1E4	data[17:0]
Set Trigger Mask for trigger block 7$^{(p)}$	18	RW	0x1F4	data[17:0]

Table 7: List of additional commands defined for the Master MACTRIS via VME registers 0xY4 and 0x1Y4, where Y=0 thru F.

downloading the firmware into the FPGA or sending a VME firmware reset, it it set to a default value of 470 (0x1d7) 8ns clock samplings.

(f) This register defines the length of the LIVE gate, starting from the leading edge of the START NIM signal, in units of the 8 ns clock ticks. Upon downloading the firmware into the FPGA or sending a VME firmware reset, it is set to a default value of 0x2000000, which corresponds to about 4 s.

(g) These registers define the value of the energy threshold used to compare against the calorimeter total and daisy-chain calorimeter energy sum: 0x7c for the total, 0x9c for the left daisy-chain and 0xbc for the right daisy-chain energy. Upon downloading the firmware into the FPGA or sending a VME firmware reset, they are set to a default value of 0x3FFFF. The18 bits of the "high" energy sum threshold are defined mapping bit(31:18) of register 0x7c into the 14 MSB and constraining the 4 LBS to be all zeros. Upon downloading the firmware into the FPGA or sending a VME firmware reset, it is are set to a default value of 0x3FFF0.

(h) By writing 1 to bit(0) of register 0xac, the logic to generate L1As inside the L1A_MANAGER block is re-enabled after the maximum number of triggers allowed for the spill, L1A_MAX, has been reached. This maximum value is set by register 0xd4. Upon downloading the firmware into the FPGA or sending a VME firmware reset, L1A_MAX is set to 10752 (0x2A00). When L1A_MAX is reached, bit(1) of status register 0xec goes high.

(i) Register 0x14 sets a 10-bit mask which specifies which of the 8 internal triggers or of the 2 external triggers will generate an automatic L2A. This information is passed to the L2 Trigger system via the length of the L1A signal. The default length of the L1A signal is 3 clks, which is interpreted by the L2 Trigger as a request to analyze the Center-Of-Energy of the event before making a L2A decision. For events for which we require an automatic L2A decision, the L2A_MANAGER block drives the AUTO_L2_ENABLE signal high, to which the L1A_MANAGER block responds by issuing a 5 clks long L1A [7]. The L2A_MANAGER drives AUTO_L2_ENABLE high if at least one internal or external trigger has fired and such trigger is allowed to generate an automatic L2A as encoded in bits(9:0) of register 0x14 (bit(7:0) for internal triggers and bit(9:8) for external triggers, respectively.) By writing 0 to bit(19) of register 0xcc, we disable AUTO_L2_ENABLE and allow bit(20) of register 0xcc to simulated the automatic L2A. The default value for both bit(19) and bit(20) is zero, meaning that the automatic L2A based on the L2A_MANAGER is disabled and the length of the L1A is 3 clk cycles. The status of the automatic L2A decision, either from the L2A_MANAGER or simulated, can be seen on bit(8) of register 0xec.

(j) By setting bit(27) of register 0xcc high, we generate triggers at a random rate while LIVE is high. The rate of these random triggers is controlled by the "Set Random Trigger Rate" register 0xc4, which defines the threshold above which a 32-bit random sequence will generate a trigger. Typical values are: 0xFFFF0000 for $\approx$ 1KHz, 0xFFFFC000 for $\approx$ 4KHz, 0xFFFF8000 for $\approx$ 8KHz and 0xFFFF6000 for $\approx$ 10KHz. Any value above this

[7] The length of L1A is decoded inside the ADC firmware, which sets bit(9) of the first COE word to 1 if the COE decision has to be overridden

makes the behavior of the random generator unstable and it is not recommended. Upon downloading the firmware into the FPGA or sending a VME firmware reset, the default value for register 0xc4 is 0xFFFFFFFF. The default value for bit(27) of 0xcc is 0.

(k) By setting bit(28) of register 0xcc high, we allow the loss-of-sync condition to disable any further L1 trigger until the end of the spill. The loss-of-sync is generated by comparing the TLK errors generated by any L1 Trigger board against a maximum value set by register 0xb4. The loss-of-sync condition can be monitored via bit(5) of register 0xec. TLK errors detected in any L1 Trigger boards are connected to the K0TO_ERROR line, which is a negative logic Open Collector signal of the P2 backplane. This signal is routed via the L1 Trigger crate Slave MACTRIS to input A_K0TO_ERROR of the Master MACTRIS. A_K0TO_ERROR enables a TLK error counter when bit(30) of register 0xcc is set high and its status can be monitored via bit(7) of register 0xec. Upon downloading the firmware into the FPGA or sending a VME firmware reset, both bit(28) and bit(30) of register 0xcc are set to 0 while the maximum number of TLK errors is set to 32 (0x20).

(l) By setting bit(29) of register 0xcc high, we enable multiple consecutive L1A in response to a "Simulate L1A to ADC" command, i.e. writing register 0x3c to 1. The number of L1As and the gap between them, in units of 8 ns clock ticks, is set by the bit(15:0) and bit(31:16) of register 0xa4, respectively. Upon downloading the firmware into the FPGA or sending a VME firmware reset, the default value for register 0xa4 is 0x1000001. The default value for bit(29) of 0xcc is 0.

(m) By setting bit(31) of register 0xcc high, we prevent `disable_l1a` from being set (see Figure reffig:l2a). `disable_l1a` is a temporary disable of L1A triggers during the spill. Two conditions can generate this limited blackout: the INPUT_BUFFER_L2_SIM simulator detecting a condition of almost full L2 input buffers (`input_fifo_full`); or the L2 Trigger board reporting an interrup request because the 2GB memory is temporary unavailable for writing more data (`L2_irq`). The first condition corresponds to the L2 input buffers having accumulated 10(7) L1 triggers with 48(64) samplings without any L2A decision. It can be monitored via bit(4) of register 0xec. The number of ADC samplings is passed to the INPUT_BUFFER_L2_SIM block via VME register 0x24 (see note (s)). The second condition is generated by the Virtex 4 on the L2 Trigger board, when its firmware detects an "almost full" condition on the internal fifo writing to the 2Gb memory. In response to this, the L2 Trigger boards drives the K0TO_ERROR line, which is a negative logic Open Collector signal of the P2 backplane. This signal in turn is routed via the L2 Trigger Crate Slave MACTRIS to input B_K0TO_ERROR of the Master MACTRIS firmware. Its status can be monitored via bit(7) of register 0xec. The default value for bit(31) of register 0xcc is 1.

(n) By writing 1 to bit(0) of these registers we reset different parts of the firmware. More specifically, 0x4c resets all of the counters to zero, 0xdc clears the contents of the FIFOs and 0xfc resets all of the VME controlled registers to their default value.

(o) By writing 1 to bit(27) of 0xcc we enable the L2A input to the INPUT_BUFFER_L2_SIM. L2A is generated by the L2 Trigger board after an event has been analyzed for the L2 decision (see Figure **??**). In response to this, any L2 Trigger board can pull down the

Open Collector K0TO_NOT_EMPTY signal of the P2 backplane. This signal in turn is routed via the L2 Trigger Crate Slave MACTRIS to input B_K0TO_NOT_EMPTY of the Master MACTRIS firmware. . To protect from spurious L2A, we disable this input to INPUT_BUFFER_L2_SIM for 1024 clk cycles after one L2A is observed.

(p) This register enables the outputs from the 8 YASU_TRIGGER_LOGIC blocks into the internal L1 trigger OR decision as raw trigger bits, before prescale (see Figure 3). The default value for all of the enables is zero, in which case a L1 trigger can still be generated via VME as a single trigger (see note *d*), as multiple equidistant triggers (see note *l*) or as random triggers (see note *j*). The internal triggers can be bypassed when making the L1 decision by writing 1 to bit(6) of register 0xcc to zero (default value is 1). The internal and external triggers can be bypassed when making the L1 decision by writing 1 to bit(7) of register 0xcc to zero (default value is 0). The inputs to the YASU_TRIGGER_LOGIC BLOCK are enabled according to an 18 bits mask (see Figure 4), whose definition is summarized here: TRG_MASK(2:0) are reserved for the calorimeter triggers TRG_MASK(3)=0 for the spare input and TRG_MASK(15:4) for the veto triggers; two special high-level control masks, TRG_MASK(16) and TRG_MASK(17), determine whether the calorimeter and veto inputs are used in coincidence (TRG_MASK(16)=1) or anti-coincidence (TRG_MASK(16)=0), and whether the veto input is the AND (TRG_MASK(17)=0 with TRG_MASK(16)=1) or the OR (TRG_MASK(17)=1 with TRG_MASK(16) = 0) of all enabled veto triggers.

(q) This bit monitors the status of the ERROR signal generated by any ADC board. When running with VME readout, the ERROR line is used to signify that all of the ADC boards are done reading the triggers in their internal memory and L1A can be issued again. ERROR rising edge generates MAX_L1A_CLR which, analogously to bit(1) of register 0xac (see note (h)), is used to re-enable the generation of L1As inside the L1A_MANAGER block. Note that when using VME readout, the maximum number of 64 sample triggers (L1A_MAX via register 0xd4) is set to 42 (0x26). For ERROR to be active, bit(3) of register 0xcc has to be set to 0. If set to 1, ERROR can still be simulated via VME by writing 1 to bit(11) of register 0xcc. The default value for bit(3) is 1 and for bit(11) is 0, which assume L2 readout is used.

(r) This register checks the length of the L2 decision signals coming to Master MACTRIS via the B_K0TO_DONE input. A signal longer/shorter that a number of clock cycles set by bit(7:0) signifies that the L1A trigger has been accepted/reject by the COE cut, that is it has received a L2A/L2R decision. Upon downloading the firmware into the FPGA or sending a VME firmware reset, it is set to a default value of 16 (0x10) clock cycles. The L2A_R is validates by the L2A signal (see *m*) and can be driven by any L2 Trigger board using the OC K0TO_DONE P2 backplane signal. The rising edge of L2A_R is used to read trigger diagnostics from L1 FIFOs containing every L1A triggers. When the L2A_R stretches past the number of clock cycles set by register 0x154, the diagnostic info for the trigger at the output of the L1 FIFOs is written into the L2 FIFOs.To avoid reflections around the L2A_R signal, we avoid picking up any other activity on the line carrying this signals for 10 clock cycles at both the rising and falling edges.

(s) This register changes the number of ADC samplings to be used by the input FIFO simulator logic INPUT_BUFFER_L2_SIM module. Upon downloading the firmware into the

FPGA or sending a VME firmware reset, it is set to a default value of 48 (0x30). Only allowed values are 48, 56, 64 and 72. Any attempt to download a value different from these will result in the register going back to its default value. **The other action required when setting the number of ADC samplings to a value different from the default is to change the L1A_MAX (register 0xD4) that controls the maximum number of trigger fragments fitting in the 2Gb memory: 0x2400 for 56 samplings, 0x1E00 for 64 samplings and 0x1C00 for 72 samplings.**

(t) These registers set independent delays for the veto bits after they have been received from the P2 backplane and before they are gated and used in the L1 trigger decision. Each register controls the delay for 4 veto signals according to the following scheme: bit(4:0) for the first of the 4 veto bits, bit(12:8) for the second, bit(20:16) for the third and bit(28:24) for the fourth. The default value for all of delays is zero.

(u) This register sets the delay for the different variables used in the CsI trigger calculation: bit(4:0) is for the sum of the energy before the threshold comparison, bit(12:8) is for the left daisy-chain, bit(20:16) for the right daisy-chain energy before the threshold comparison and bit(28:24) is for the crate-sum trigger decision. The default value for all of the delays is zero.

(v) These registers sets the length of the veto and crate sum trigger gates to be used in coincidence with the CsI trigger for the final L1A decision. For the veto triggers, each of registers 0x104, 0x204 and 0x304 set the length for 4 different veto detectors using bit(7:0), but(15:8), bit(23:16) and bit(31:24), respectively. The ensuing VETO_GATE(11:0) signals are connected to the VETO(11:0) inputs of the YASU_TRIGGER_LOGIC block. For the crate sum trigger, bit(7:0) of register 0x74 set the length of CSUM_GATE starting from the first sampling for which the sum of the CSUM goes over the a programmable threshold. This threshold is set by bit(3:0) of register 0x144. Only CSUM triggers enabled by register 0x134 go into the sum. The CSUM_GATE is then connected to the CSUM_TRG input of the YASU_TRIGGER_LOGIC block. A second CSUM1_GATE was connected to the SPARE_TRG input of the YASU_TRIGGER_LOGIC block. It was generated using a second minimum number of CSUM triggers defined via bit(19:16) of register 0x144. Upon downloading the firmware into the FPGA or sending a VME firmware reset, the default value for all of the gate lengths is 1. Finally, bit(23:16) of register 0x74 are used to set the width of the time window for the data saved in the VETO_FIFO, which monitors the time evolution of each veto and energy peak triggers in proximity of the L1A trigger (see Section 5).

(w) These registers sets the prescale factors for the outputs of the 8 YASU_TRIGGER_LOGIC blocks before OR-ing them for the internal L1 decision. These prescales just set the number of triggers to ignore before accepting one for the internal L1 decision. Each register control the prescales for two outputs via bit(15:0) and bit(31:16), respectively. The prescale is done inside the PRESCALER module with a clock latency of 2. A prescale of 1 leaves the signal rate unchanged. **A prescale of zero sets the output always high.** Upon downloading the firmware into the FPGA or sending a VME firmware reset, the default value of 1 is set for all of the prescale factors.

(x) The MSB 16 bits of register 0xec carry information about the board and firmware, namely bit(19:16) encode a unique value of the MACTRIS type (0xC for Master MACTRIS, 0xE for COE a and 0xF for Slave); bit(23:20) and bit(27:24) encode the firmare version and revision number; but(31:28) encode a unique value for each trigger board in the system (0x1 for L1 Trigger, 0x2 for L2 Trigger, 0x4 for MACTRIS)

(y) Bit(6) of register 0xec monitors the status of the OC K0TO_FULL P2 backplane signal connected to the Slave MACTRIS in the L2 Trigger crate. This signal, connected to the B_K0TO_FULL input of the Master MACTRIS firmware, is driven by any L2 Trigger board which sees either an interrupt request from the Virtex 4 FPGA or detects that any of its input buffers are full.

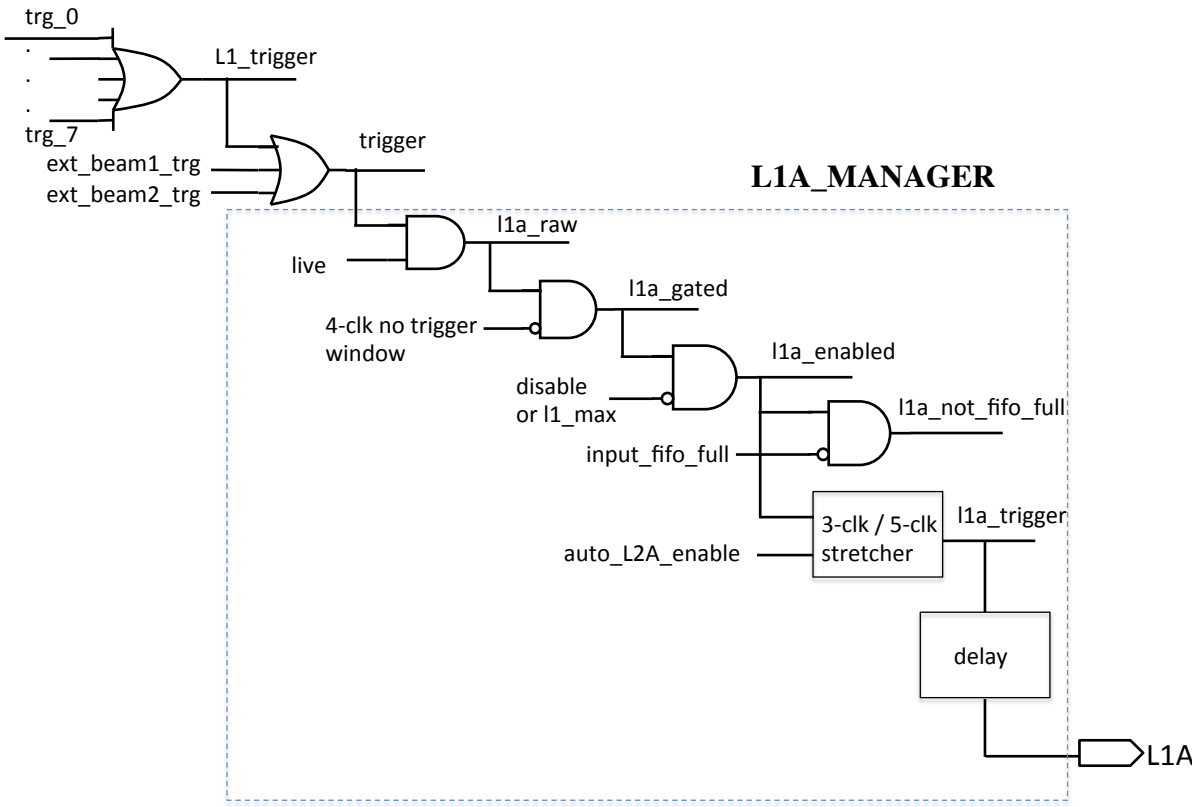

Figure 6: L1 Triggers at different steps of the L1A decision.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read Left Daisy Chain E_{SUM}	24	RO	0x8	data[23:0]
Read Right Daisy Chain E_{SUM}	24	RO	0x18	data[23:0]
Read L+R Daisy Chain E_{SUM}	24	RO	0x28	data[23:0]
Read Total "Low" E_{SUM} peak counter	32	RO	0x38	data[31:0]
Read Right E_{SUM} peak counter	32	RO	0x48	data[31:0]
Read Left E_{SUM} peak counter	32	RO	0x58	data[31:0]
Read CSUM peak counter	32	RO	0x68	data[31:0]
Read `l1a_trigger` counter	32	RO	0x78	data[31:0]
Read `l1a_enable` trigger counter	32	RO	0x88	data[31:0]
Read `l1a_raw trigger` counter	32	RO	0x98	data[31:0]
Read `l1a_not_fifo_full` trigger counter	32	RO	0xA8	data[31:0]
Read `ext_beam2_trg` counter	32	RO	0xB8	data[31:0]
Read `L1_trigger` counter	32	RO	0xC8	data[31:0]
Read `ext_beam1_trg` counter	32	RO	0xD8	data[31:0]
Read `int_L1trg` trigger counter	32	RO	0xE8	data[31:0]
Read `trigger` decision counter	32	RO	0xF8	data[31:0]
Read veto bit(0) counter	32	RO	0x00	data[31:0]
Read veto bit(1) counter	32	RO	0x10	data[31:0]
Read veto bit(2) counter	32	RO	0x20	data[31:0]
Read veto bit(3) counter	32	RO	0x30	data[31:0]
Read veto bit(4) counter	32	RO	0x40	data[31:0]
Read veto bit(5) counter	32	RO	0x50	data[31:0]
Read veto bit(6) counter	32	RO	0x60	data[31:0]
Read veto bit(7) counter	32	RO	0x70	data[31:0]
Read veto bit(8) counter	32	RO	0x80	data[31:0]
Read veto bit(9) counter	32	RO	0x90	data[31:0]
Read veto bit(10) counter	32	RO	0xa0	data[31:0]
Read veto bit(11) counter	32	RO	0xb0	data[31:0]
Read CSUM1 peak counter$^{(v)}$	32	RO	0x148	data[31:0]
Read L2A counter	32	RO	0x158	data[31:0]
Read L2R counter	32	RO	0x168	data[31:0]
Read Total "High" E_{SUM} peak counter	32	RO	0x178	data[31:0]

Table 8: List of VME registers used to read the counters of input triggers to YASU_TRIGGER_BLOCK, L1 triggers at different stages of the L1A decision (see Figure 3 and 6 for a signal legend) and L2A/L2R decisions.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
Read unprescaled trigger 0 counter	32	RO	0x100	data[31:0]
Read unprescaled trigger 1 counter	32	RO	0x110	data[31:0]
Read unprescaled trigger 2 counter	32	RO	0x120	data[31:0]
Read unprescaled trigger 3 counter	32	RO	0x130	data[31:0]
Read unprescaled trigger 4 counter	32	RO	0x140	data[31:0]
Read unprescaled trigger 5 counter	32	RO	0x150	data[31:0]
Read unprescaled trigger 6 counter	32	RO	0x160	data[31:0]
Read unprescaled trigger 7 counter	32	RO	0x170	data[31:0]
Read prescaled trigger 0 counter	32	RO	0x180	data[31:0]
Read prescaled trigger 1 counter	32	RO	0x190	data[31:0]
Read prescaled trigger 2 counter	32	RO	0x1A0	data[31:0]
Read prescaled trigger 3 counter	32	RO	0x1B0	data[31:0]
Read prescaled trigger 4 counter	32	RO	0x1C0	data[31:0]
Read prescaled trigger 5 counter	32	RO	0x1D0	data[31:0]
Read prescaled trigger 6 counter	32	RO	0x1E0	data[31:0]
Read prescaled trigger 7 counter	32	RO	0x1F0	data[31:0]
Read CSUM trg delay for slots 4,5,6,9	32	RO	0xc0	data[31:0]
Read CSUM trg delay for slots 10,11,13,14	32	RO	0xd0	data[31:0]
Read CSUM trg delay for slots 15,18,19,20	32	RO	0xe0	data[31:0]
Read Left E_{SUM} trigger delay	8	RO	0x108	data[7:0]
Read Right E_{SUM} trigger delay	8	RO	0x108	data[15:8]
Read L+R E_{SUM} trigger delay	8	RO	0x108	data[23:16]
Read CSUM trigger delay	8	RO	0x108	data[31:24]
Read veto bit 0 trigger delay	8	RO	0x118	data[7:0]
Read veto bit 1 trigger delay	8	RO	0x118	data[15:8]
Read veto bit 2 trigger delay	8	RO	0x118	data[23:16]
Read veto bit 3 trigger delay	8	RO	0x118	data[31:24]
Read veto bit 4 trigger delay	8	RO	0x128	data[7:0]
Read veto bit 5 trigger delay	8	RO	0x128	data[15:8]
Read veto bit 6 trigger delay	8	RO	0x128	data[23:16]
Read veto bit 7 trigger delay	8	RO	0x128	data[31:24]
Read veto bit 8 trigger delay	8	RO	0x138	data[7:0]
Read veto bit 9 trigger delay	8	RO	0x138	data[15:8]
Read veto bit 10 trigger delay	8	RO	0x138	data[23:16]
Read veto bit 11 trigger delay	8	RO	0x138	data[31:24]

Table 9: List of VME registers used to read the number of triggers observed before and after prescaling each of the signals connected to the 8-input OR gate used in the `L1_trigger` decision. The trigger delay counters measure the number of 8 ns clk it takes from LIVE to those signals being first seen inside the MACTRIS firmware during the initial calibration.

4 FIFO Registers

Master MACTRIS firmware exchange signals with the Trigger boards in the L1 and L2 Crates via the P2 and P3 backplane. Tables 10 and 11 list such signals, together with their source or destination. A brief description follows. Signals with † symbol are used for COE protocol and exchanged between COE MACTRIS and the Trigger boards in the L2 Crate.

Name	Destination	Description
CLK125_DAQ	all boards	System Clock, copy on on-board 125 MHz Oscillator
L1A_BKPLN	all boards	L1A Trigger
LIVE_BKPLN	all boards	Extended LIVE Gate
L2A_EN	all L2TRG boards	L2 decision has been $^{(\dagger)}$
L2A	all L2TRG boards	L2A decision if HIGH, L2R decision if LOW$^{(\dagger)}$
KOTO_RSVD	all L2TRG boards	Enable COE data into L2TRG P3 backplane$^{(\dagger)}$
Name	**Source**	**Description**
A_K0TO_ERROR	Any L1TRG board	TLK Errors above threshold$^{(h)}$
B_K0TO_FULL	Any L2TRG board	Any Input FIFO is predicted to be full$^{(m)}$
B_K0TO_DONE	Any L2TRG board	L2R/L2A if shorter/longer than 16 clks$^{(r)}$
B_K0TO_ERROR	Any L2TRG board	L2 memory is full$^{(m)}$
B_K0TO_RSVD_OC	Any L2TRG board	L2 memory is full$^{(m)}$

Table 10: List of P2 signals driven (top) or received (bottom) by the Master MACTRIS firmware. Signals identified with a † symbol are exchanged only L2 Trigger crate P2 backplane.

Name	Source	Description
K0TO_PTP1	L1TRG boards in Daisy Chain	Regional Calorimeter Trigger
K0TO_PTP1	L2TRG boards in Daisy Chain	COE FIFO has data$^{(\dagger)}$
K0TO_PTP2	L2TRG boards in Daisy Chain	COE data SENT to P3$^{(\dagger)}$

Table 11: List of P3 signals received by the Master MACTRIS (top) and COE MACTRIS (bottom) firmware.

5 FIFO Registers

The FIFOs inside the Master MACTRIS firmware have a monitoring function by collecting trigger and detector status data at or around the time when a trigger is issued. The data is then read out via VME in between spills and added to the data stream offline. With the advent of the L2 trigger based COE, all of the monitoring FIFOs had to be mirrored by a second FIFO, generically called L1_L2_FIFO, which is written when L1A is issued and readout out when the L2A_L2R signal arrives from the L2 Trigger (see igure 7). If the L2A_L2R signal is decoded as being a L2A signal, i.e. longer than 16 clks, the data in the L1_L2_FIFO is copied in the final monitoring FIFO to be read out in between spills. The one exception is the TIMESTAMP_FIFO which records the time of each L1A trigger issued during the spill, with or without L2 validation.

Master MACTRIS firmware v8.0 and above implements 8 monitoring FIFOs as summarized below. Each monitoring FIFO comes with its own mirror L1_L2_FIFO of the same data width but only 32-word deep.

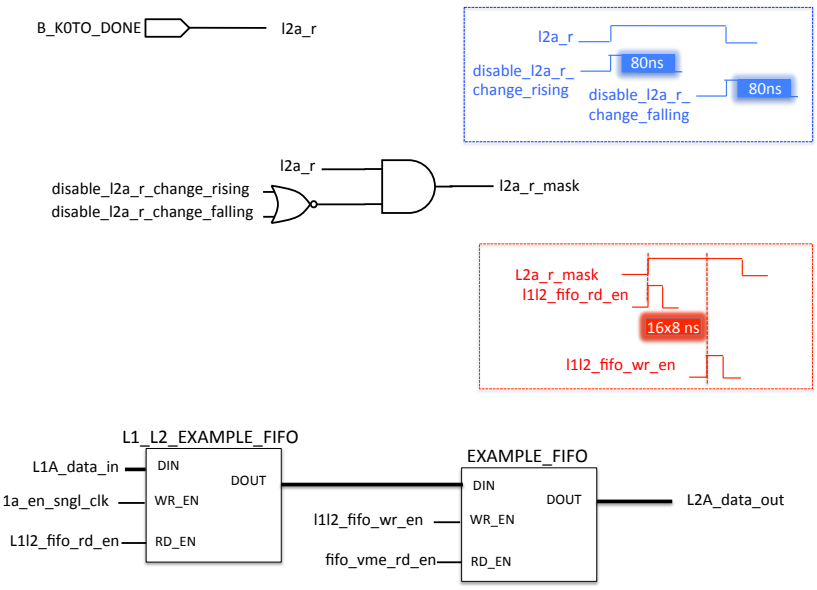

Figure 7: Details of the implementation of the write and read enable logic for the monitoring FIFOs inside the Master MACTRIS firmware. The dashed blue boxes contains the logic used to clean up the edges of the L2A_R signals from spurious hits due to reflections. The rising edge of L2A_R_MASK is used to read the content of L1_L2_FIFOs, which are the FIFO containing all of the L1A triggers while the first clock sampling for which L2A_R is longer than the minimum length required for a L2 accept, is used to write the L1A event at the output of the L1_L2_FIFO into the final diagnostic FIFO for all accepted events.

- Two 18-bit 8K deep ETSUM_FIFOs recording the Left and Right Daisy Chain E_{SUM} energy at the time when L1A is issued. These FIFOs are readout via VME register 0x1000000 and 0x1100000, respectively.

- One 16-bit 32K deep VETO_FIFO recording the time evolution of the Left Daisy-Chain veto triggers (bit(5:0)), Right Daisy-Chain veto triggers (bit(11:6)), SUM_PEAK1 trigger (bit(12)), CSUM_GATE1 trigger (bit(13)), SUM_PEAK trigger (bit(14)) and CSUM_GATE trigger (bit(15)) for time window of N clock cycles centered around the L1A, as specified by bits(23:16) of VME register 0x74 (see end of note (v). This FIFO is readout via VME register 0x1400000.

- Two 11-bit 8K deep TAG_FIFOs recording the status of individual trigger bits used in the L1A decision. In particular bit(7:0) of each FIFO contain the data at the output of the YASU_TRIGGER_LOGIC blocks before and after prescaling, bit(8) has the status of SPILL_GATE (bit(8)), and bit(9) and bit(10) rep or the status of external LVDS trigger signals, before and after the VME enable. These FIFOs are readout via VME register 0x1500000 and 0x1600000, respectively.

- One 4 bit 8K deep CSUM_FIFO recording the number of CSUM triggers, i.e. the number of regional triggers when L1A is issued. This FIFO is readout via VME register 0x1800000.

- One 18-bit 32K deep TIMESTAMP_FIFO recording the time at which L1A is issued, in units of 8 ns clocks after LIVE. Unlike the others, this monitoring FIFO is written for each L1A trigger, validated or not by the L2 decision. Bit(16:0) contain a copy of the 17 LSB of the "time from LIVE" counter (i.e. two L1A triggers 2^{17} clock cycles, or 1ms, apart will have the same timestamp) while bit(17) report whether that trigger was a L2A or a L2R. This info is used offline to correlate the monitoring FIFOs data with data saved in the normal readout stream by cross-checking the timestamp of L2A events with the timestamp written by the ADC in the header of each event. This FIFO is readout via VME register 0x1900000.

- One 16-bit 8K deep L1A_CNT_FIFO recording the running counter of L1A issued during the spill. This FIFO is readout via VME register 0x1A00000.

Name	Size	VME Access	VME Addr[31..0]	Bit Assignment
SPL NIM Input Scaler	31	RO	0xc	data[31:0]
START NIM Input Scaler(1)	31	RO	0x1c	data[31:0]
EXT_SIG_IN1 LVDS Input Scaler(1)	31	RO	0x2c	data[31:0]
EXT_SIG_IN2 LVDS Input Scaler(1)	31	RO	0x3c	data[31:0]
Send Counters Reset	1	WO	0x4c	data[0]
Set time between FIFO captures(2)	16	RW	0x8c	data[15:0]
Send FIFO Reset	1	WO	0xdc	data[0]
Read Board Flavor(3)	4	RO	0xec	data[19:16]
Read Firmware Revision	4	RO	0xec	data[23:20]
Read Firmware Version	4	RO	0xec	data[27:24]
Read Board Type(4)	4	RO	0xec	data[31:28]
Send Firmware VME Reset	1	WO	0xfc	data[0]
Read **EXT_SIG_IN1** Scaler FIFO	32	RO	0x100000	data[31:0]
Read **EXT_SIG_IN2** Scaler FIFO	32	RO	0x110000	data[31:0]

Table 12: List of of VME Control Register defined for firmware for SMACTRIS board in L1 Trigger Crate.

6 SMACTRIS VME Registers

The SMACTRIS in the L1 Trigger Crate is downloaded with a firmware that connects the SPL and START NIM inputs signals, as well as KEK RJ45 LVD input signals, to some counters and to a FIFO. It is used to monitor the status of accelerator scalers proportional to the number of protons in the beam and the number of halo particles. Table 12 lists all of the VME registers defined in the firmware for this board.

(1) These inputs are enabled by the SPL NIM signal.

(2) This register sets the frequency, in units of 8ns clock ticks starting from **SPL**, of the FIFO writes for the scalers connected to the **EXT_SIG_1** and **EXT_SIG_2** LVDS inputs. Upon downloading the firmware into the FPGA or sending a VME firmware reset, it is set to a default value of 0x40.

(3) 0xF for Master MACTRIS, 0xC for Slave MACTRIS

(4) 0x1 for L1 Trigger board, 0x2 for L2 Trigger board, 0x4 for MACTRIS.

7 Master MACTRIS Schematics Description

Sheet 1 Input Clock Logic; Heartbit and VME Activity LED Logic; NIM, Ext. Trigger and KOTO DAQ Signals I/O.

Sheet 2 VME Interface; Command Registers Logic; Firmware Version bits.

Sheet 3 LIVE Logic; ADC ERROR and MAX_L1A_CLR Logic.

Sheet 4 Daisy-Chain Delay Buffers and Simulation.

Sheet 5 Daisy-Chain Calibration Logic.

Sheet 6 ETSUM_FIFOs for monitoring Right and Left Daisy-Chain energies at L1A.

Sheet 7 Counters of internal and external triggers. L2A_Manager block.

Sheet 8 Counters of L1 trigger at different steps of L1A decision. Counters of L2A and L2R triggers. Second total energy threshold.

Sheet 9 Left/Right/Sum Energy and Veto input bits programmable delays.

Sheet 10 Energy Threshold Registers, Energy Peak Logic, Trigger Inputs Enables and Prescales.

Sheet 11 L1A Disable Logic, L1A_Manager block and Veto Monitoring FIFO.

Sheet 12 Input Veto Bit Scalers.

Sheet 13 Tag FIFOs.

Sheet 14 New Command Registers and Fixed/Random Rate Trigger Simulator.

Sheet 15 YASU_trigger_logic blocks. Disables/Prescalers for inputs to tt L1_trigger logic.

Sheet 16 L1 trigger Input Scalers.

Sheet 17 Veto Gate Logic and Timestamp FIFO.

Sheet 18 PTP Signals delays and CSUM adder.

Sheet 19 L1A Counter and CSUM Monitoring FIFOs after L1A and L2A. Regional trigger decision for two separate thresholds.

Sheet 20 Trigger Delay Calibration.

Sheet 21 Spurious L2A and L2A_R cleaner logic. L1L2_FIFOs Read and Write Enable Logic.

Sheet 22 and 23 Firmware Versioning History.